Application Note

Application with SCALE™-2 Gate Driver Cores

Single and Dual-Channel SCALE™-2 IGBT and MOSFET Driver Cores

Introduction and Overview

The SCALE™-2 IGBT and MOSFET gate driver cores are highly integrated low-cost components which provide the user with the highest level of technology and functionality for industrial and traction requirements. These features, coupled with their flexibility of design, have already made many power converters highly successful. Nevertheless, SCALE-2 gate driver cores are not plug-and-play gate drivers. A minimum understanding of power electronics is therefore necessary to develop reliable inverter systems with these cores.

This Application Note will highlight important design rules to help users and avoid qualification problems. Moreover it will help to speed up the development time by showing detailed examples about how to design SCALE-2 gate driver cores successfully.

Considered SCALE-2 gate driver cores are: **2SC0106T**, **2SC0108T**, **2SC0435T**, **2SC0650P**, **1SC2060P**, **2SC0535T**, **2SC0635T** and **1SC0450V**.

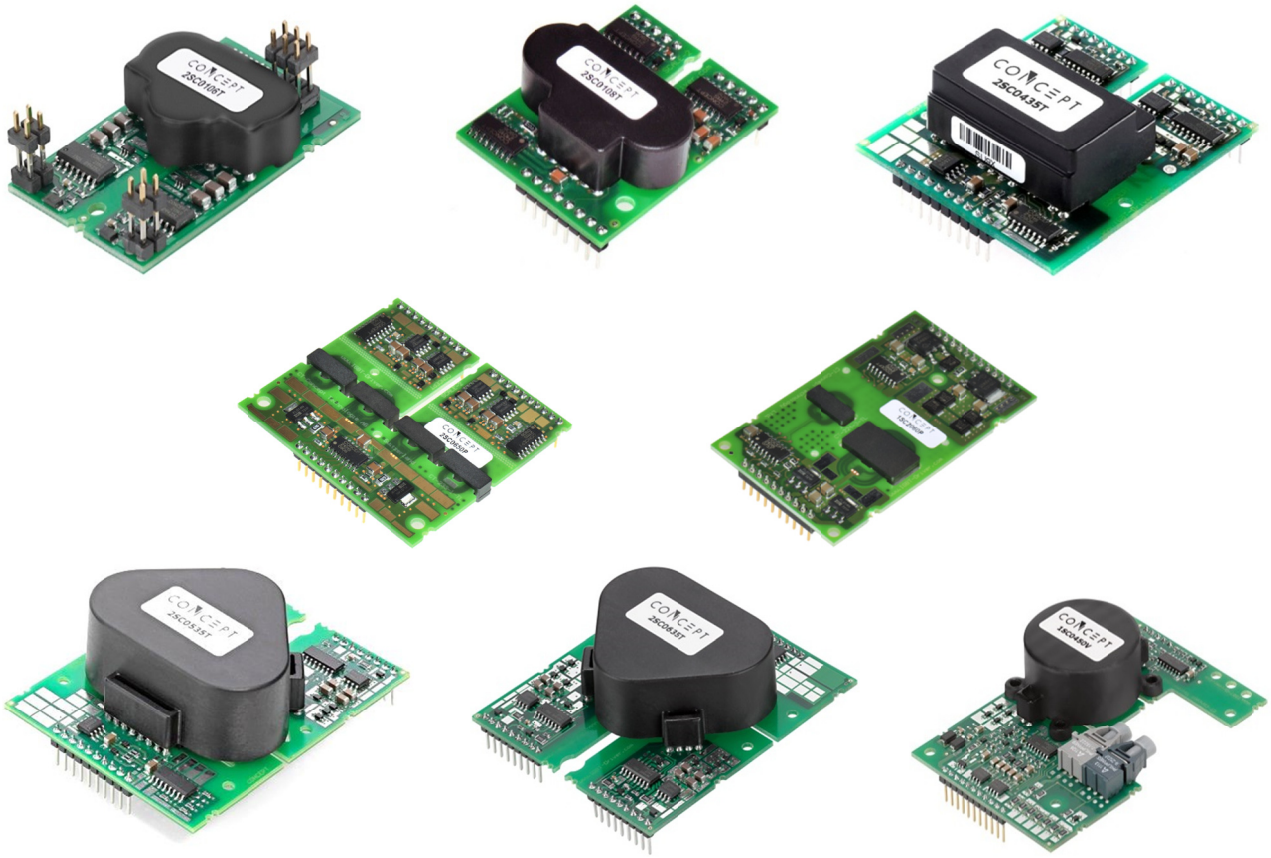

Fig. 1 SCALE-2 gate driver cores

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Applications with SCALE-2 Products

A successful use of SCALE-2 gate driver cores is coupled with an appropriate overall design. The key points listed below are success factors for the use of SCALE-2 gate drivers:

- Topology (e.g. how to parallelize IGBT modules)
- Schematics and right choice of components
- Geometrical location of IGBT gate drivers (where to place gate drivers)
- Magnetic field influences
- Clearance and creepage distances
- PCB layout
- Use of standards
- EMI considerations

SCALE-2 in Different Topologies

Use of SCALE-2 gate driver cores in three-level or multilevel topologies

During the operation of three-level converters, regular semiconductor commutation ensures that the inner IGBTs/MOSFETs are not turned off when the outer IGBTs/MOSFETs are in the on-state in order to avoid the full DC-link voltage being applied to the corresponding power semiconductors.

This situation must be considered when using CONCEPT SCALE-2 gate drivers. Such events could happen if the protection function of the gate drivers detects a short circuit or in the case of power-supply under-voltage. After fault detection, the gate driver turns the corresponding channel off immediately (exceptions are 2SC0635T and 1SC0450V, where a delay between secondary fault detection and IGBT turn-off can be programmed, see the corresponding product documentation /1/, /2/). The power semiconductors are not usually designed to withstand the full DC-link voltage. Destruction of the power semiconductor can consequently be prevented only if an adequate protection scheme is applied.

SCALE-2 Advanced Active Clamping protects the IGBTs/MOSFETs from excessive collector-emitter voltages in such situations. It therefore obviates the need to provide a dedicated turn-off sequence for the driver channels to be turned off in the fault condition - instead, the turn-off commands may be applied immediately after fault feedback. It is recommended to apply a common turn-off command to all IGBT drivers within the converter to achieve a stable system state after fault feedback.

Please also refer to Application Note AN-0901 /3/ or to the paper "Safe Driving of Multi-Level Converters Using Sophisticated Gate Driver Technology" /5/ for more information.

Note: The under-voltage protection function of the SCALE-2 chipset cannot be disabled. The gate driver channel is turned off as soon as an under-voltage event is detected on the primary or secondary side (exceptions: 2SC0635T and 1SC0450V, for which a delay can be programmed in case of a secondary-side fault). The use of active clamping consequently offers the best protection. In such cases, however, CONCEPT highly recommends testing the effectiveness of the active clamping function in the final converter design.

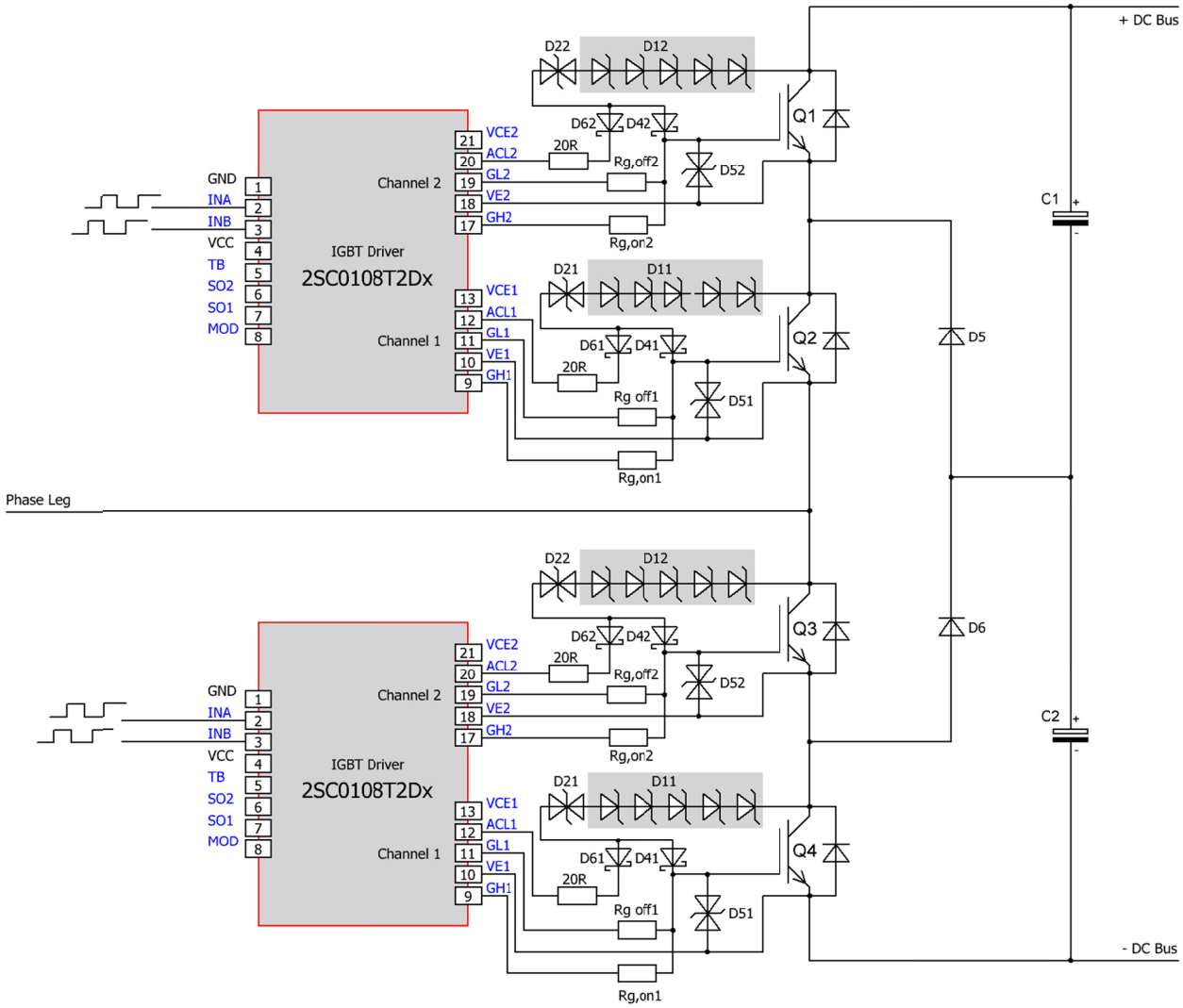

Fig. 2 Three-level converter with use of Advanced Active Clamping

Use of a single SCALE-2 gate driver for paralleled IGBTs/MOSFETs

Advanced Active Clamping in parallel IGBT operation with one common driver core

Active clamping is a technique designed to partially turn on the power semiconductor as soon as the collector-emitter (drain-source) voltage exceeds a predefined threshold. The power semiconductor is then kept in linear operation.

Basic active clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor devices (TVS) to the IGBT gate. Most SCALE-2 products support CONCEPT's Advanced Active Clamping, where feedback is also provided to the driver's secondary side at pin ACLx: As soon as the voltage on the right side of the 20Ω resistor of Fig. 3 exceeds about 1.3V, the turn-off MOSFET of the driver stage is progressively switched off in order to improve the effectiveness of the active clamping and reduce the losses in the TVS. The turn-off MOSFET is completely switched off when the voltage on the right side of the 20Ω resistors approaches 20V (measured with respect to COMx). In parallel IGBT operation with the use of only one driver core, Advanced Active Clamping needs to control all parallel-connected IGBTs/MOSFETs. A separate feedback to every gate is required according to Fig. 3.

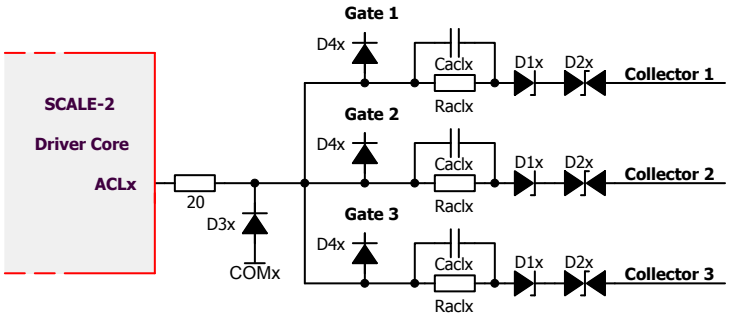

Fig. 3 Active clamping by paralleling three IGBTs/MOSFETs with one common gate driver core

It is recommended to use the circuit shown in Fig. 3 for parallel operation with one gate driver core (exceptions: 2SC0635T and 1SC0450V, for which D_{3x} and the 20Ω resistors are already included in the driver core and therefore need not be used externally). For dimensioning the TVS, R_{aclx}, C_{aclx}, D_{3x} and D_{4x}, please refer to the corresponding application manual /1/. Note that at least one of the series connected TVS must be of bidirectional type.

V_{CEsat} in parallel operation with one driver core

In general, CONCEPT recommends the use of only one V_{CEsat} detection circuit by using only one central gate driver core for paralleled IGBTs/MOSFETs, as this is sufficient to efficiently protect the system. The V_{CEsat} detection is connected to one of the parallel-connected IGBTs/MOSFETs. All paralleled IGBTs desaturate at the same time in the short-circuit condition. The maximum short-circuit current is limited by the IGBTs.

It is not recommended to connect auxiliary collectors of paralleled high-side IGBTs, as:

- A large offset current may flow and
- oscillations may occur.

Moreover, the measurement of over-current via the V_{CEsat} detection is not recommended.

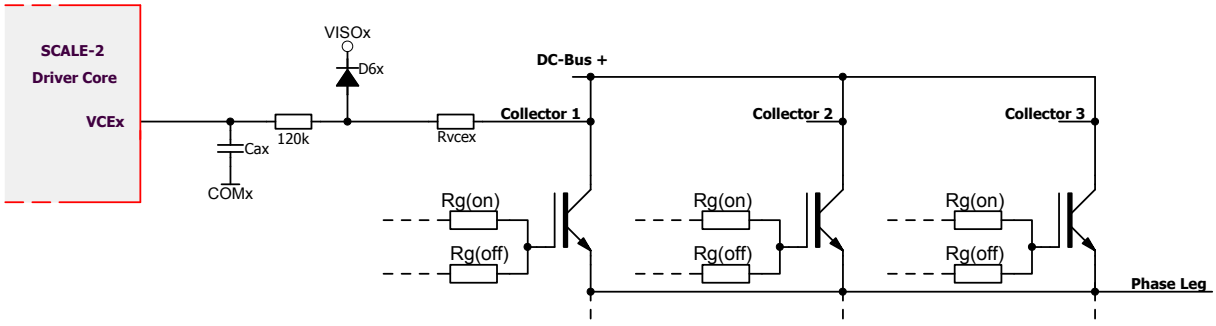

Fig. 4 V_{CEsat} detection by paralleling three IGBTs with one gate driver core

Direct paralleling

Parallel-connected IGBTs are conventionally driven by a common driver, with individual gate and emitter resistors for each IGBT (see last paragraph). An alternative approach for driving parallel-connected IGBT modules is to use an individual driver for each module (direct paralleling). This driving option is available for all driver cores with electrical interface considered in this Application Note.

If direct paralleling of SCALE-2 drivers is required, please refer to the Application Note AN-0904 /4/.

Application Note

Application Circuits

Minimum pulse suppression for inputs INA and INB

SCALE-2 gate drivers with electrical interface feature very fast signal propagation delays of typically <90ns. This includes a minimum pulse suppression time of 35ns. To avoid false gate switching caused by potential EMI, the inputs INA and INB may be equipped with additional filters. Fig. 5 illustrates how to increase the minimum pulse suppression time for driver cores with electrical interface if the SCALE-2 internal minimum suppression time is not long enough.

Fig. 5 shows that it is not recommended to apply a RC network directly to INA or INB as the jitter of the propagation delay may increase considerably. The use of a Schmitt-trigger is recommended to avoid this drawback.

Note that it is recommended to parallel the inputs INA/INB of the drivers after the Schmitt-trigger inverters if direct paralleling is used together with minimum pulse suppression. The use of a Schmitt-trigger inverter for each driver core is not recommended by direct paralleling as the delay divergence of the Schmitt-trigger inverters may be too high, leading to an excessive dynamic current imbalance during IGBT commutation.

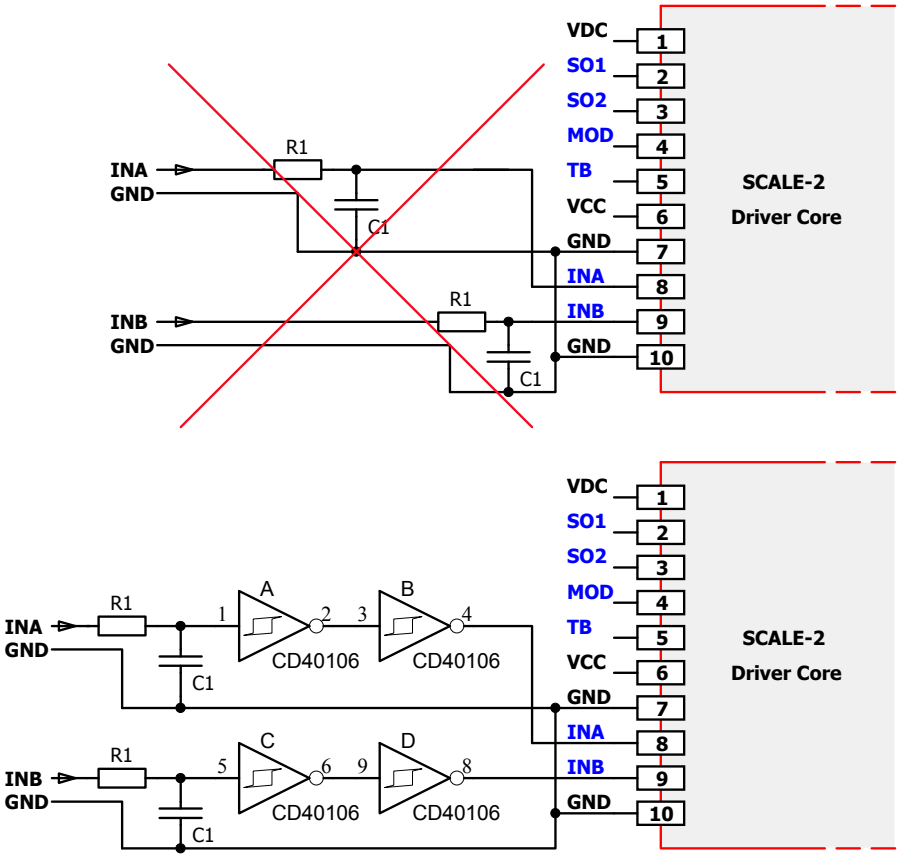

Fig. 5 Minimum pulse suppression for INA and INB for SCALE-2 driver cores

The R_1/C_1 combination together with a 15V Schmitt-trigger inverter CD40106 create minimum pulse suppression. As an example, the Schmitt-trigger input hysteresis is 5V if the turn-on level is 10V and the turn-off level is 5V. If INx turns on with 15V logic, the capacitor C_1 is charged by R_1. When the voltage across C_1 reaches 10V, the Schmitt trigger switches. If INx becomes low (turn-off command) and the voltage across the

capacitor C_1 falls below 5V, the Schmitt trigger switches. In the example, which uses two Schmitt-trigger inverters, the input signals do not need to be inverted.

The minimum pulse suppression time $T_{min,on}$ at turn-on can be calculated as follows:

$$T_{\min,on} = R_1 \cdot C_1 \cdot \ln\left(\frac{V_{DD}}{V_{DD} - V_{TH,high}}\right) \quad \text{Eq. 1}$$

where $V_{TH,high}$ is the upper Schmitt-trigger threshold and V_{DD} is the logic level of INx.

The minimum pulse suppression time $T_{min,off}$ at turn-off can be calculated as follows:

$$T_{\min,off} = R_1 \cdot C_1 \cdot \ln\left(\frac{V_{DD}}{V_{TH,low}}\right) \quad \text{Eq. 2}$$

where $V_{TH,low}$ is the lower Schmitt-trigger threshold and V_{DD} is the logic level of INx.

Example:

- $T_{min,on}$=500ns: R_1=3.3kΩ, $V_{TH,high}$=10V, VDD=15V, C_1= 138pF
- $T_{min,off}$=1µs: R_1=3.3kΩ, $V_{TH,low}$=5V, VDD=15V, C_1= 276pF

Increase of the noise immunity at inputs INA and INB (excluding 2SC0635T)

Most SCALE-2 gate driver cores with electrical interface turn on the corresponding channel when INA/INB reaches a threshold voltage of about 2.6V (exception: 2SC0635T). The turn-off threshold voltage is about 1.3V, resulting in a hysteresis of 1.3V. In some applications with very high noise interference voltages (EMI), or when long cables are used, increasing the input threshold voltage helps to avoid irregular switching events. For this purpose, a voltage divider R_2/R_3 is placed as close as possible to the gate driver core according to Fig. 6. The minimum distance between the voltage divider R_2/R_3 and the gate driver is essential to avoid inductive coupling on the PCB layout.

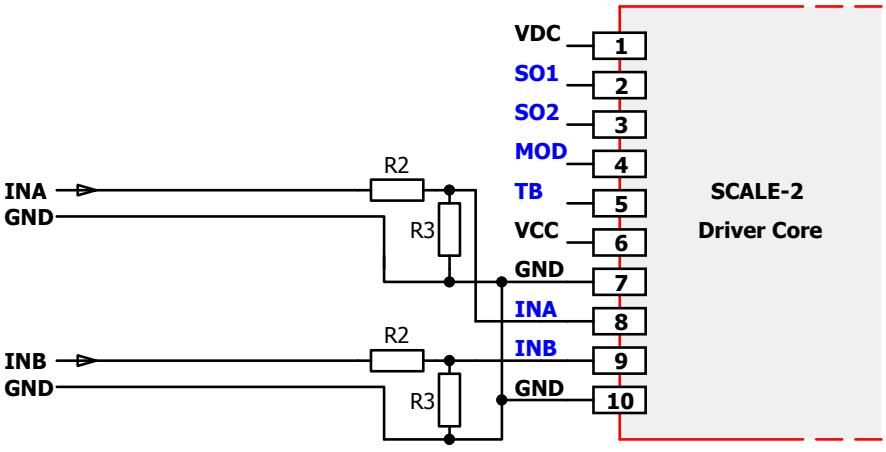

Fig. 6 Increased threshold voltages INA and INB with SCALE-2 gate driver cores

Example: Setting R_2=3.3kΩ, R_3=1kΩ and INA=15V at turn-on. Without R_2 and R_3, the gate driver turns on as soon as INA reaches 2.6V. The voltage divider increases the turn-on threshold voltage to about 11.2V. The turn-off threshold voltage is now about 5.6V. In this example, the INA and INB signal drivers have to provide 3.5mA during the IGBT on-state.

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Use of external optical interface with SCALE-2 gate drivers with internal electrical interface

For applications requiring optical PWM inputs and fault outputs, CONCEPT products permit different solutions. Beside standard plug-and-play driver solutions for high-voltage IGBTs and the driver core 1SC0450V, an alternative solution is to just use an optical interface in front of a SCALE-2 IGBT gate driver core with an electrical interface. Fig. 7 shows an example of how to drive a SCALE-2 driver core with a standard AVAGO HFBR type (for other manufacturers, e.g. TOSHIBA, PANASONICS, … contact the CONCEPT support service). A Schmitt trigger CD40106 (supplied with 5V) inverts the output signal of the HFBR-2522ETZ into a 5V logic signal. This signal drives the SCALE-2 gate driver core. The open drain fault outputs SO1 and SO2 have a 1kΩ pull-up resistor to drive the optical interface. The light is on during the normal condition and off in the fault condition. The diode current during normal operation is about 15mA. During the fault condition, this current flows via open drain SO1 and/or SO2, respectively. The maximum allowed SO1/SO2 load current is 20mA.

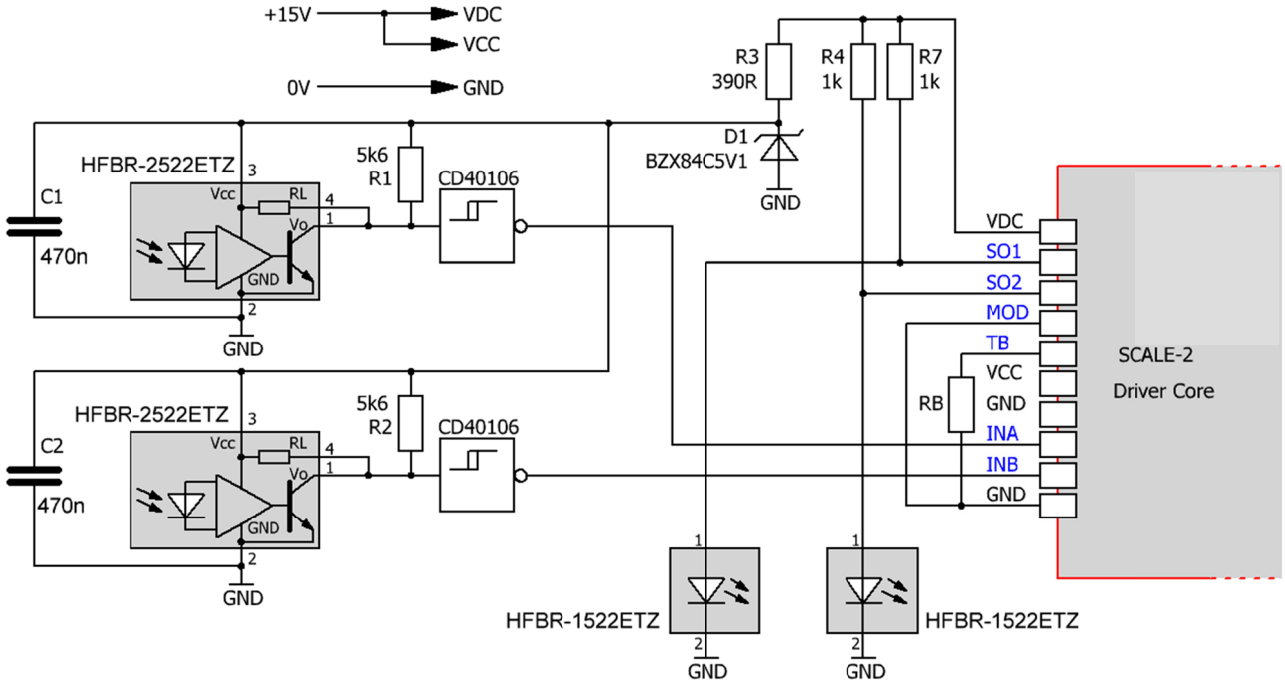

Fig. 7 Optical interface driving a SCALE-2 gate driver core

Only direct mode is recommended (MOD is connected to GND) with the use of two or more SCALE-2 gate driver cores with direct paralleling (Fig. 8). The inputs INA and INB of each driver are connected in parallel. The SOx fault outputs can be connected together or each can be wired to a fiber-optics interface. A pull-up resistor must be placed as close as possible to the gate driver core. This resistor is calculated for a diode current of approximately 13mA and a maximum open collector current of 20mA per channel.

Note that both pins TB are paralleled. The resistor value of R_B given in the data sheet /2/ must therefore be divided by two to obtain the corresponding blocking time. The power supply of CD40106 must be 5V.

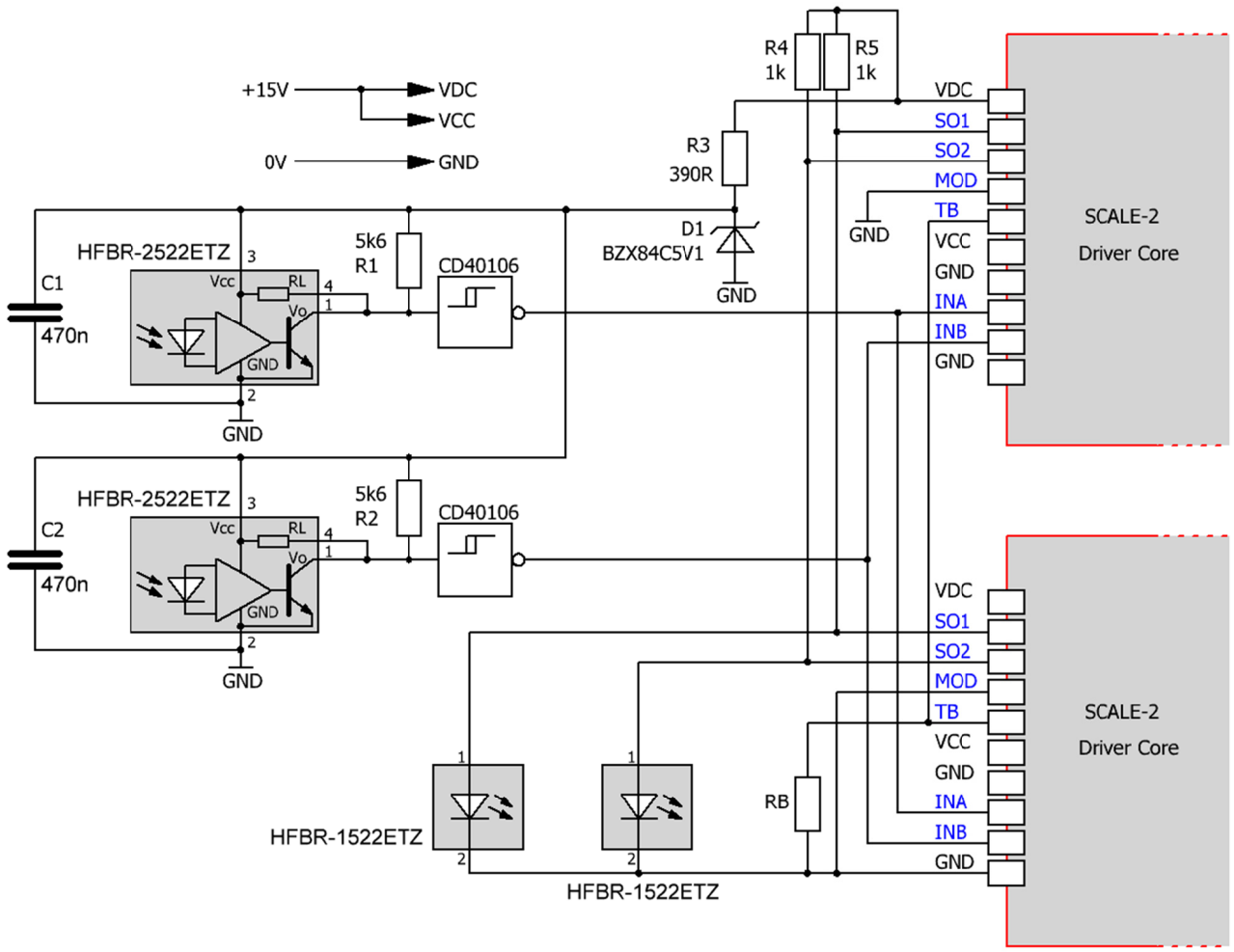

Fig. 8 Optical interface driving paralleled SCALE-2 gate driver cores (example with 2SC0435T)

Note that both circuits of Fig. 7 and Fig. 8 cannot be used with 2SC0635T, as the input thresholds of INA and INB are higher (adjustment for 15V logic required).

Half-bridge mode

The MOD pin – if available – can be used to configure direct or half-bridge mode on dual-channel drivers (see corresponding application manual /1/ for more information).

It is recommended to place the components R_m and C_m (see corresponding application manual /1/) as close as possible to the MOD pins and to avoid big loops.

The dead time tolerance may vary from product to product and from the dead time setup and is also dependent on the target PCB layout. A tolerance of approximately ±15% may be expected.

Moreover, it is impermissible to change between direct and half-bridge mode, or the reverse during driver operation. This may result in high-frequency burst pulses that may destroy the driver.

External implementation of half-bridge mode

Dead times between both channels of a driver core can also be generated with external circuitry using the direct mode of the SCALE-2 driver. This can be useful if the required dead time length is outside the range provided by the SCALE-2 technology (about 0.6-4.1µs) or when higher timing precision is needed.

The PWM pattern, including the required dead times, can be generated using digital circuits (e.g. µP, FPGAs, CPLDs) or with external circuits. Fig. 9 below shows a circuit example that generates dead times in a similar way as the SCALE-2 technology, using an enable signal and a switching signal.

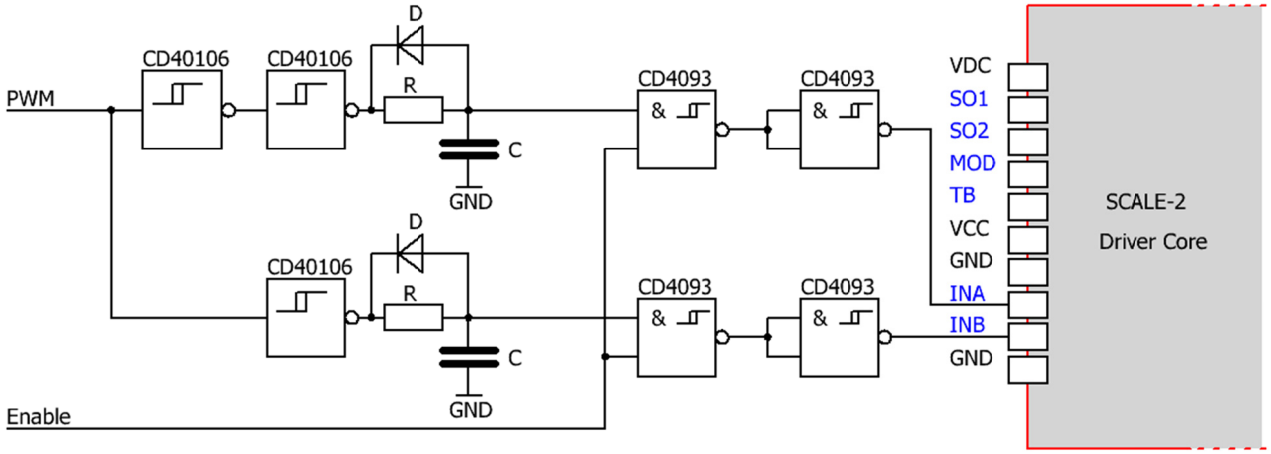

Fig. 9 Recommended circuit for the external generation of half-bridge dead times

The required dead times T_D can be approximately set up with the components R and C considering the thresholds of the NAND gates used:

$$T_D \approx R \cdot C \cdot \ln\left(\frac{V_{DD}}{V_{DD} - V_{TH,high}}\right) \qquad \text{Eq. 3}$$

where $V_{TH,high}$ is the upper Schmitt-trigger threshold and V_{DD} is the logic level of the Schmitt-trigger inverters/NAND gates, that may be 5V…15V. It is recommended to use high-speed switching diodes for the diodes D.

Example: A half-bridge dead time of $T_D \approx 7.7$µs can be set up with R=4.7kΩ and C=1.5nF (V_{DD}=15V, $V_{TH,high}$=10V)

External implementation of minimum channel interlock time

When dead times are generated externally using the direct mode of the SCALE-2 driver cores, it is possible to implement an interlock circuit according to Fig. 10 that avoids simultaneous switching of the inputs/outputs, even if the generated switching signals are incorrect.

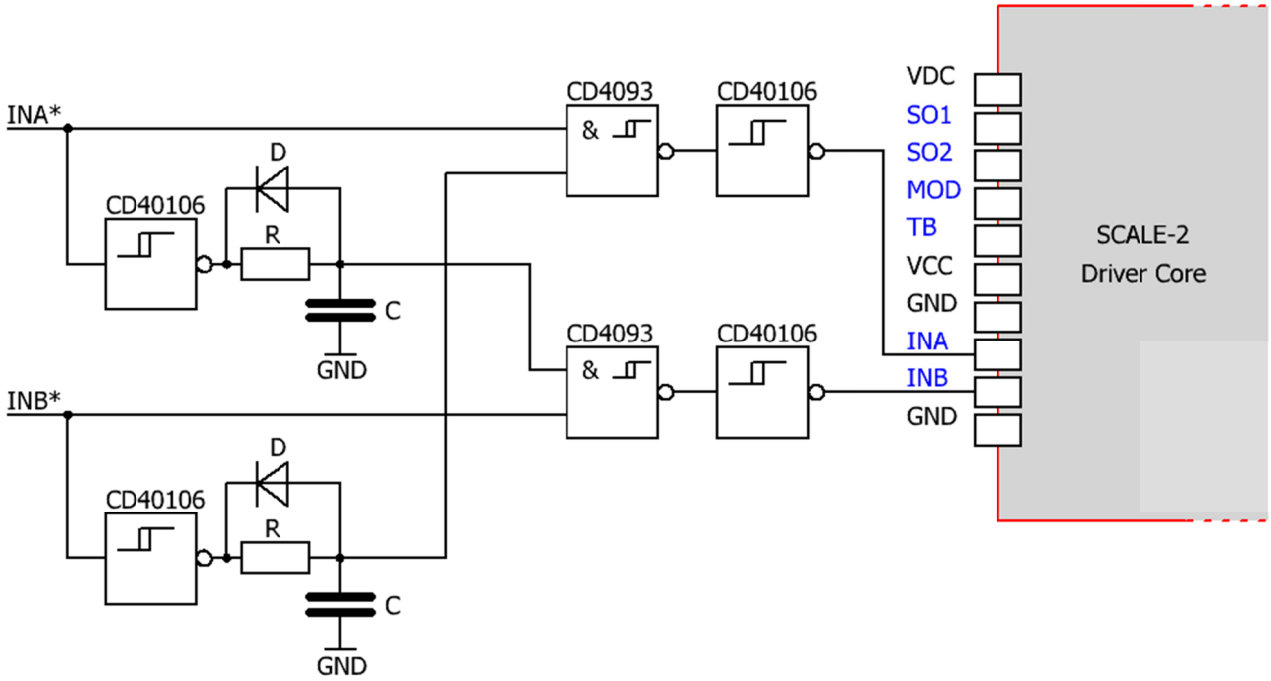

Fig. 10 Recommended circuitry for setting a minimum interlock time

The circuit shown in Fig. 10 does not significantly modify the switching signals INA* and INB* if the minimum programmed interlock time T_I is not undercut:

$$T_I \approx R \cdot C \cdot \ln\left(\frac{V_{DD}}{V_{DD} - V_{TH,high}}\right) \qquad \text{Eq. 4}$$

where $V_{TH,high}$ is the upper Schmitt-trigger threshold and V_{DD} is the logic level of the Schmitt-trigger inverters/NAND gates, that may be 5V…15V. It is recommended to use high-speed switching diodes for the diodes D.

If the signals INA* and INB* have a dead time which is lower than the programmed minimum interlock time T_I, the dead time between both channels is automatically extended to T_I.

If both signals INA* and INB* are high at the same time, both channels are turned off.

Note that the use of external components increases the overall propagation delay time of the gate driver.

Use of SOx fault outputs

The longer the distance to the microcontroller, the more EMI-sensitive does the SOx line become. When no fault condition is detected, the SOx output has high impedance. Voltage spikes can therefore easily be induced.

CONCEPT recommends the use of the circuit shown in Fig. 11 if long cable distances are necessary or if the SOx current capability of 20mA is not sufficient. The MOSFETs T11/T12 protect the driver's SOx outputs from EMI influences. It is additionally recommended to use pull-down resistors on the host controller cable side to

provide safe logic in case the SOx signal should not be connected properly (e.g. broken cable). Note that the pull-down resistor values must not be too low, as a voltage divider is built with the MOSFET pull-up resistors.

The SOx driving current can be easily increased by reducing the 2.7k pull-up resistor values of the MOSFETs.

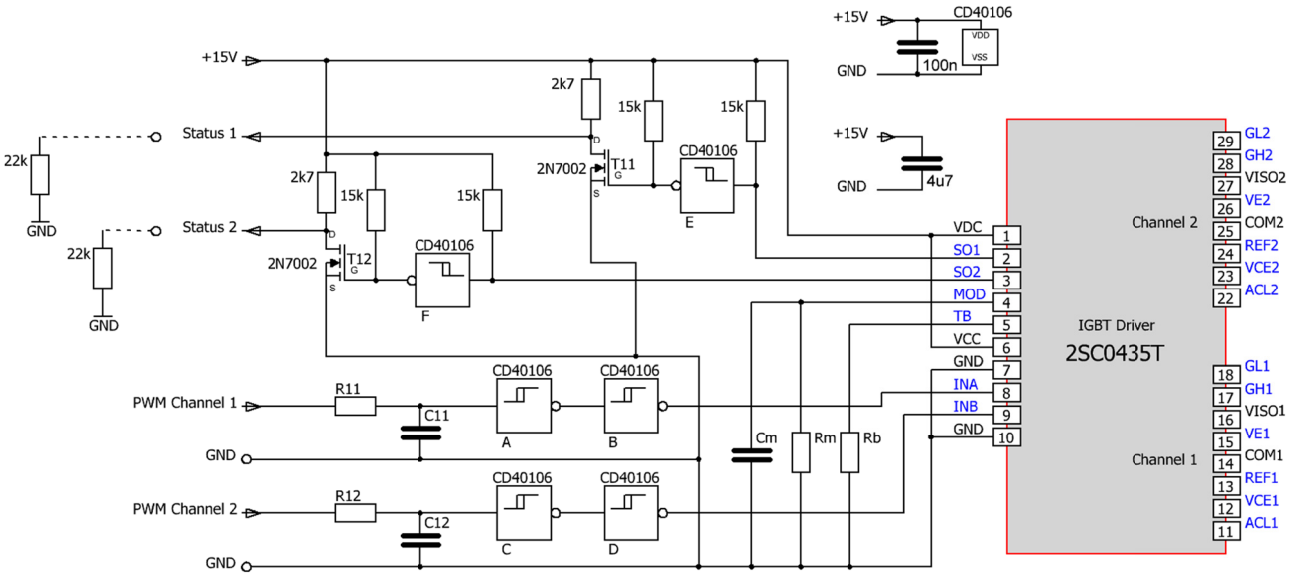

Fig. 11 Use of SOx fault signals over long distances

Note that a protection circuit for the SOx pins as well as a pull-up resistor of 10kΩ is available on the driver cores 2SC0635T and 1SC0450V.

Use of gate resistors

Most of the SCALE-2 driver cores feature separated paths GHx and GLx to connect the turn-on and turn-off gate resistors. It is mandatory to use separated turn-on and turn-off gate resistors, as shown in Fig. 12. Increased power losses and oscillations may occur if GHx is directly connected to GLx. However, this does not apply to 2SC0106T.

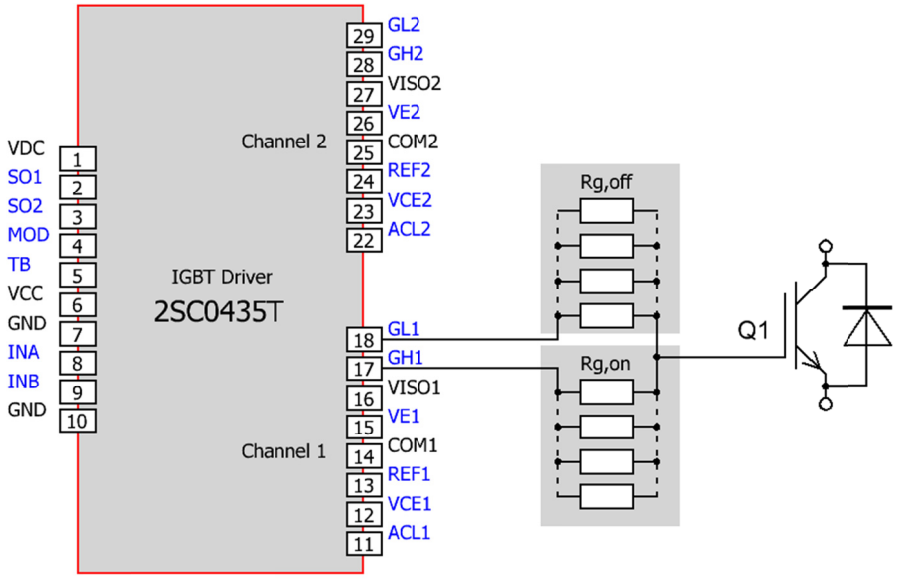

Fig. 12 Use of gate resistors with the terminals GHx and GLx

Moreover, it is necessary for several reasons to keep the inductance of the gate loop as small as possible:

- High gate-loop inductances will alter the switching performance of the IGBT. In particular, faster commutation may occur during turn-on, which could cause SOA violation of the corresponding free-wheeling diode.
- The use of high-inductance resistors (e.g. wire wound resistors) is impermissible. It is recommended to use high-power proofed 1206 SMD resistors (e.g. CRCW1206 resistors from Vishay) or leaded metal film resistors (e.g. PR02 or PR03 from Vishay) and to measure the temperature increase of the gate resistors at the target switching frequency to avoid thermal overload. A maximum temperature increase of 40K or lower is usually recommended. Moreover, the peak power capability of the gate resistors must not be exceeded.
- Reducing the gate loop inductance reduces possible coupling from external magnetic fields into the gate circuit. Such coupling may alter the gate driver performance, generate oscillations or even lead to the IGBT SOA being exceeded under certain circumstances. If possible and/or required, shielding planes can be used to reduce the influence of external magnetic fields.

VEx terminal characteristics

VEx corresponds to the emitter potential. It is an internally generated potential of the SCALE-2 ASIC. During normal operation, the voltage between the pins VISOx and VEx is regulated to a nominal value of 15V. This is done by means of a SCALE-2 internal current source and voltage measurement in the secondary ASIC IGD. Its maximum sink/source capability is limited to ±2.5mA in order to avoid thermal overloading of the ASIC during operation.

If the secondary voltage between VISOx and COMx begins to fall, the voltage between VISOx and VEx remains constant at 15V in a first step. The voltage between VEx and COMx is reduced up to about 5.5V. If the voltage still falls from VISOx to COMx, the voltage from VEx to COMx remains constant at 5.5V and the voltage from VISOx to VEx begins to fall. This function ensures a proper turn-off of IGBTs even in the event of a supply under-voltage.

No static load should be applied between VISOx and VEx or between VEx and COMx in order not to disturb the 15V regulation between VISOx and VEx. A static load can be applied between VISOx and COMx if necessary (e.g. supply load for external electronic functions). This is illustrated in Fig. 13.

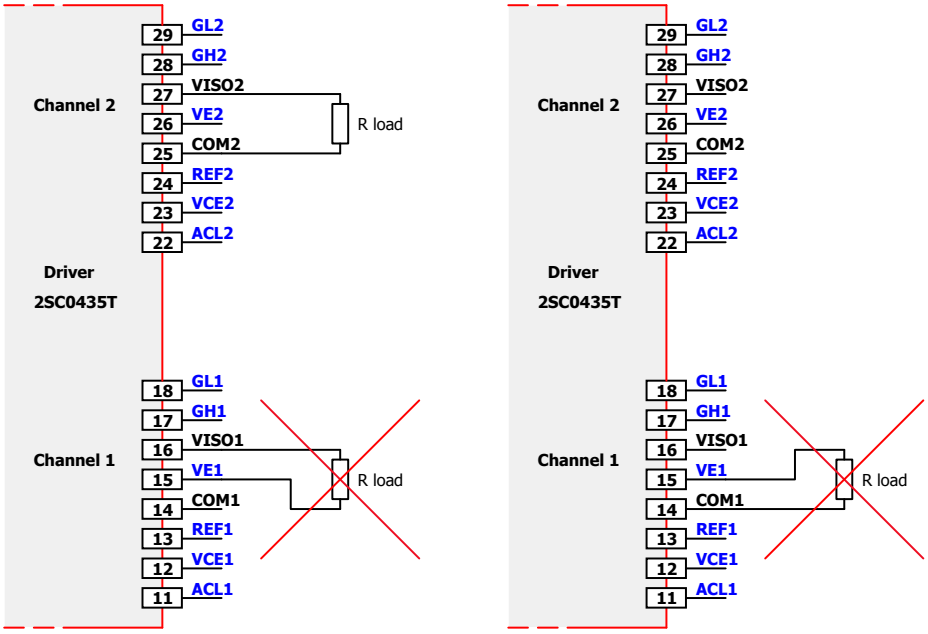

Fig. 13 External loading of VISOx, VEx and COMx (example with 2SC0435T)

Note that it is not permitted to insert a resistor between the gate and emitter as shown in Fig. 14, as this would also statically load the 15V regulator.

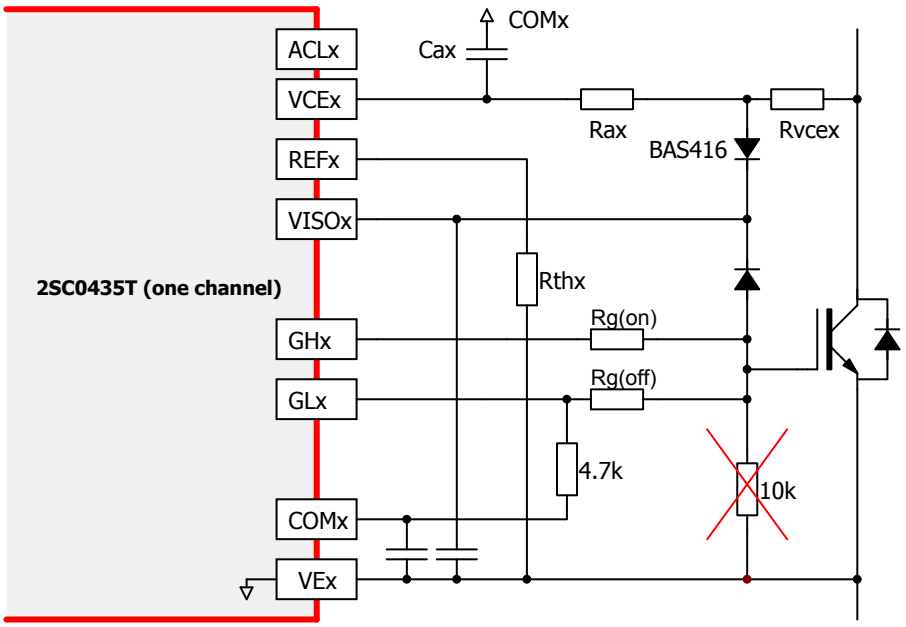

Fig. 14 Impermissible resistor between gate and emitter (example with 2SC0435T)

The voltage at VEx (and therefore the gate-emitter voltage) can also be set to a specific custom value by means of external circuitry. The internally controlled 2.5mA DC current at VEx is then drawn/sourced by external components such as a combination of a resistor with a Zener diode or by a linear regulator. When realizing deviating voltage levels with external circuitry, several points have to be observed:

- The voltage between VISOx and VEx as well as VEx and COMx must not exceed 20V.
- The voltage between VISOx and VEx as well as VEx and COMx must not be set to a value which triggers the under-voltage monitoring (UVLO). For specific values, refer to the respective data sheet /2/ for the gate driver. The exception is MOSFET mode (see section "MOSFET mode (not available on 2SC0106T and 2SC0108T)").
- It is impermissible to switch VEx to COMx potential when the driver is supplied with power.

If voltage levels that violate the above rules are required, please contact the CONCEPT support service.

Required blocking capacitors C_{1x} and C_{2x}

The SCALE-2 gate drivers are equipped with blocking capacitors on the secondary side of the DC/DC converter (for values, refer to the corresponding driver data sheet /2/). These blocking capacitors allow fast charging and discharging of the gate capacitance of power semiconductors (which is characterized by the gate charge) via the N-channel MOSFET driver stages.

For IGBTs or MOSFETs, a minimum total blocking capacitance of 3µF is recommended for every 1µC of gate charge, unless otherwise specified in the corresponding application manual /1/. The missing blocking capacitance on a SCALE-2 driver core must be added externally.

The blocking capacitors must be placed between VISOx and VEx (C_{1x} in Fig. 15) as well as between VEx and COMx (C_{2x} in Fig. 15). They must be connected as close as possible to the driver's terminal pins with minimum inductance. It is recommended to use the same capacitance value for both C_{1x} and C_{2x} (IGBT mode). Ceramic capacitors with a dielectric strength >20V are recommended. Note that during power-on, the capacitors are charged with a limited current thanks to the soft start function implemented in the SCALE-2 gate drivers.

If the required capacitances C_{1x} or C_{2x} exceed the maximum value given in the corresponding description and application manual /1/, please contact CONCEPT's support service.

Note that the use of electrolytic capacitors such as tantalum capacitors is not recommended.

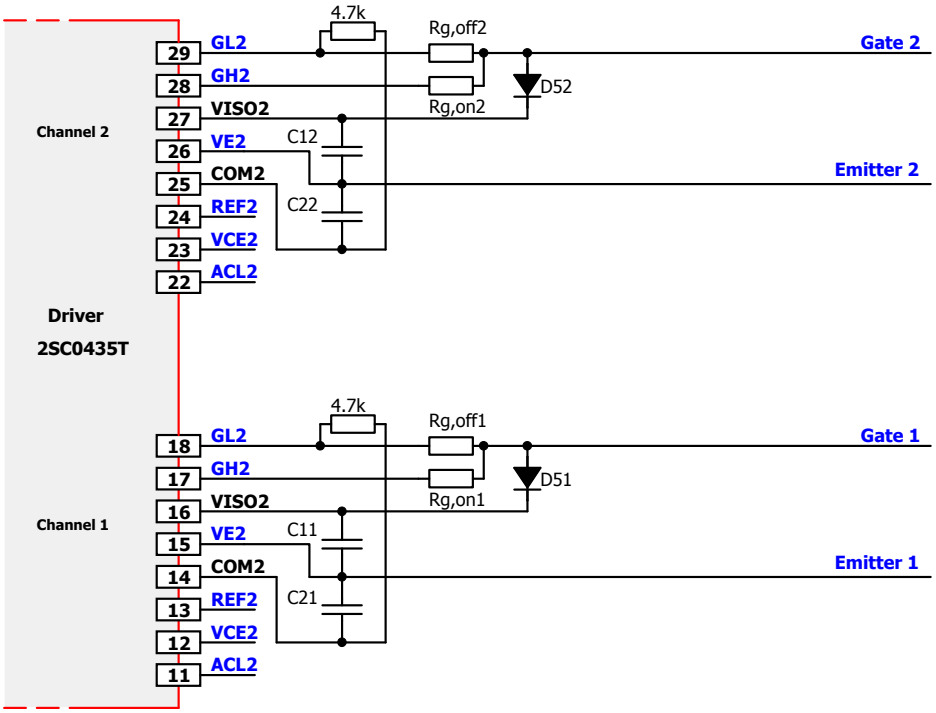

Fig. 15 Use of external blocking capacitors on the secondary side (example with 2SC0435T)

V_{CEsat} detection with SCALE-2 gate driver cores (excluding 2SC0108T)

Desaturation protection with resistors (for 650V-1700V driver cores)

The collector sense must be connected to the IGBT collector or MOSFET drain with the circuit shown in Fig. 16 and Fig. 17 in order to detect an IGBT or MOSFET short-circuit.

During an IGBT off-state, the driver's internal MOSFET connects pin VCEx to pin COMx. The capacitor C_{ax} is then pre-charged/discharged to the negative supply voltage, which is about -10V referred to VEx (red circle in Fig. 16). During this time, a current flows from the collector (blue circle in Fig. 16) via the resistor network and the diode BAS416 to VISOx. The current is limited by the resistor chain.

It is recommended to dimension the resistor value of R_{vcex} in order to obtain a current of about I_{Rvcex}=0.6-1mA flowing through R_{vcex} (e.g. 1.2-1.8MΩ for $V_{DC-LINK}$=1200V). A high-voltage resistor as well as series-connected resistors may be used. It must be ensured that the resistors R_{vcex} are not overloaded in either voltage or thermal respects:

- A maximum temperature increase of 40K or lower is usually recommended in the worst case condition.
- The maximum voltage withstand capability of the resistors used must not be exceeded. Moreover, the minimum creepage distance relating to the application must be considered.

$$I_{Rvcex} = \frac{(V_{CEx} - VISOx)}{R_{VCEx}} \qquad \text{Eq. 5}$$

The reference voltage is set by the resistor R_{thx}. It is calculated via the reference current (typically 150uA) and the reference resistance R_{thx} (green circle in Fig. 16)

$$V_{refx} = 150\mu A \cdot R_{thx}$$ Eq. 6

CONCEPT recommends the use of R_{thx}=68kΩ to detect short-circuits. Lower resistance values make the system more sensitive and do not provide any advantages in the case of desaturated IGBTs (short-circuit). Note that the resistor R_{thx} is already available on some driver cores such as 2SC0106T, 2SC0108T2D0-07, 2SC0108T2D0-12, 2SC0635T and 1SC0450V.

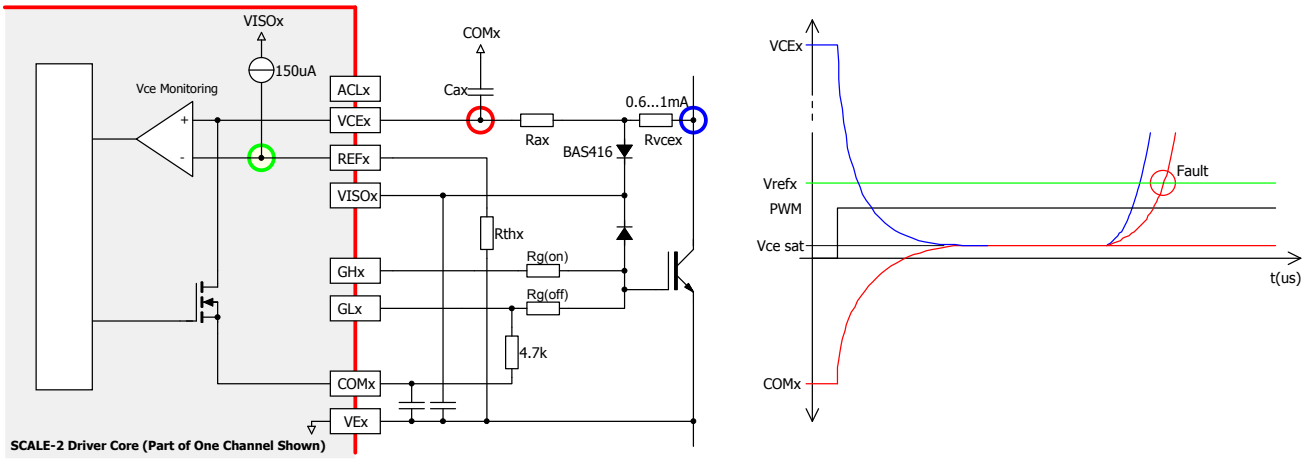

Fig. 16 V_{CE} desaturation protection with resistors (600V-1700V IGBT modules)

At IGBT turn-on and in the on-state, the above-mentioned MOSFET turns off. While V_{CE} decreases (blue curve in Fig. 16), C_{ax} is charged from the COMx potential to the IGBT saturation voltage (red curve in Fig. 16). The time required to charge C_{ax} depends on the DC bus voltage, the value of the resistor R_{ax} and the value of the capacitor C_{ax}. For 1200V and 1700V IGBTs it is recommended to set R_{ax}=120kΩ. For 600V IGBTs the recommended value is R_{ax}=62kΩ. The resulting response time is given in the corresponding application manual /1/. It is valid in the short-circuit condition for a minimum DC-link voltage of about 25V*R_{vcex}/R_{ax}. Note that the response time will increase for lower DC link voltages. However, the energy dissipated in the IGBT in the short-circuit condition generally remains at the same level or is even lower.

The diode D_1 in Fig. 17 must have a very low leakage current (in particular at elevated ambient/junction temperatures) and a blocking voltage >40V (e.g. BAS416). Schottky diodes must be explicitly avoided.

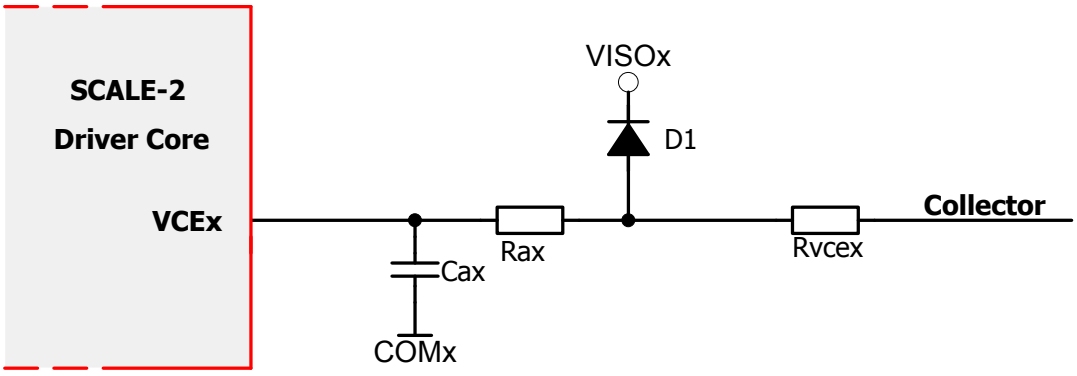

Fig. 17 Recommended circuit for desaturation protection with resistors (600V-1700V IGBT modules)

Note: The related components C_{ax}, R_{ax}, R_{thx} and D_1 must be placed as close as possible to the driver. A large collector-emitter loop must also be avoided. See the layout proposal of 2BB0435T:

www.igbt-driver.com/go/2BB0435T

It is recommended to implement a response time (short-circuit time) which is high enough to avoid false tripping of the desaturation protection during IGBT turn-on. If the desaturation protection function is set up with an insufficiently long response time, a fault may be triggered during IGBT turn-on, especially in cases where the V_{CE} voltage drop time is low (usually at high DC-link voltages, high collector currents and junction temperatures). The ruggedness of the design can be tested in the following way:

- The IGBT must be turned on at the highest DC-link voltages, collector current and junction temperature (e.g. using the double pulse technique).
- If no fault is generated, the sensitivity of the desaturation protection function can be increased by reducing the capacitance value of C_{ax} and/or reducing the driver supply voltage VDC. This allows the design margin to be checked.
- Alternatively, the turn-on speed of the IGBT module can be artificially reduced by increasing the turn-on gate resistance to check the design margin.

If the design margin is insufficient, it is recommended to increase the response time. Note, however, that the maximum allowed short-circuit time of the IGBT module must not be exceeded under the conditions stated in the data sheet of the IGBT module (if in doubt, please consult the supplier of the IGBT module).

For driver cores of voltage classes higher or equal to 3300V, the recommended circuit for desaturation protection can be found in the corresponding application manual /1/.

Desaturation protection with sense diodes (only for 650V-1700V driver cores)

SCALE-2 technology also provides desaturation protection with high-voltage diodes as shown in Fig. 18. However, the use of high-voltage diodes has some disadvantages compared to the use of resistors:

- Common-mode current relating to the rate of change dv_{ce}/dt of the collector-emitter voltage: High-voltage diodes have large junction capacitances C_j. These capacitances in combination with the dv_{ce}/dt generate a common-mode current I_{com} flowing in and out of the measurement circuit.

$$I_{com} = C_j \cdot \frac{dv_{ce}}{dt} \qquad \text{Eq. 7}$$

- Price: High-voltage diodes are more expensive than standard 0805/150V or 1206/200V SMD resistors.
- Availability: Standard thick-film resistors are comparatively easier to source on the market.
- Limited robustness: The reaction time does not increase at lower V_{CE} levels. Consequently, false triggering may occur at higher IGBT temperatures, higher collector currents, resonant switching or phase-shift PWM, particularly when the reference voltage V_{thx} is set lower than about 10V. The upper limit of the reference voltage is restricted to about 10V, which may lead to limited IGBT utilization: the collector current may be limited to values smaller than twice the nominal current, or the short-circuit withstand capability may be reduced.

During the IGBT off-state, D_4 (and R_{ax}) sets the VCEx pin to COMx potential, thereby pre-charging/discharging the capacitor C_{ax} to the negative supply voltage, which is about -10V referred to VEx. At IGBT turn-on, the capacitor C_{ax} is charged via R_{ax} to 15V. When the IGBT collector-emitter voltage drops below that value, the voltage of C_{ax} is limited via the high-voltage diodes D_1 and D_2. The voltage across C_{ax} can be calculated by:

$$V_{cax} = V_{CEsat} + V_{F(D1)} + V_{F(D2)} + (330\Omega \cdot \frac{(15V - V_{CEsat} - V_{F(D1)} - V_{F(D2)})}{(R_{ax} + 330\Omega)}) \qquad \text{Eq. 8}$$

The reference voltage V_{refx} needs to be higher than V_{cax}. It is set up by the resistor R_{thx} and can be calculated via the reference current (typically 150uA) and the reference resistance R_{thx}:

$$V_{refx} = 150\mu A \cdot R_{thx} \qquad \text{Eq. 9}$$

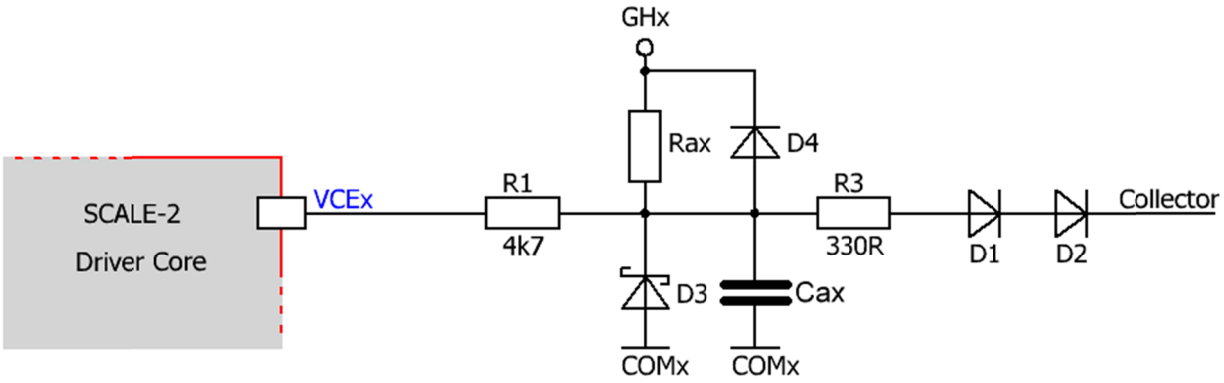

Fig. 18 Recommended circuit for desaturation protection with sense diodes

It is recommended to use standard rectifier diodes such as 1N4007 for D_1 and D_2 (2 diodes for 1200V IGBTs, 3 diodes for 1700V IGBTs). D_3 and D_4 must be high-speed diodes (e.g. BAS316). Schottky diodes must be avoided.

The value of the resistance R_{ax} can be calculated with the following equation in order to program the desired response time T_{ax} at turn-on:

$$R_{ax}[k\Omega] \approx \frac{1000 \cdot T_{ax}[\mu s]}{C_{ax}[pF] \cdot \ln\left(\frac{15V + |V_{GLx}|}{15V - V_{refx}}\right)} \qquad \text{Eq. 10}$$

V_{GLx} is the absolute value of the turn-off voltage at the driver output. It depends on the driver load and can be found in the driver data sheet /2/.

Recommended high-voltage diodes D_1/D_2 and values for R_{ax} and C_{ax} are:

- High-voltage diodes: 1x 1N4007 for 650V IGBTs
  2x 1N4007 for 1200V IGBTs
  3x 1N4007 for 1700V IGBTs
- R_{ax}=24kΩ…62kΩ
- C_{ax}=100pF…560pF

Note that C_{ax} must include the parasitic capacitance of the PCB and the diode D_3.

Note also that the instantaneous V_{CE} threshold voltage is determined by the voltage at pin REFx (150µA through R_{thx}) minus the voltage across the 330Ω resistor as well as the forward voltages across D_1 and D_2.

Note that the minimum off-state duration should not be shorter than about 1µs in order not to significantly reduce the response time for the next turn-on pulse.

Example: A resistor of R_{ax}≈46kΩ must be used to define a response time of 6µs with C_{ax}=150pF, R_{thx}=33kΩ and V_{GLx}=9V.

It is recommended to implement a response time (short-circuit time) which is high enough to avoid false tripping of the desaturation protection during IGBT turn-on. If the desaturation protection function is set up with an insufficiently long response time, a fault may be triggered during IGBT turn-on, especially in cases where the V_{CE} voltage drop time is low (usually at high DC-link voltages, high collector currents and junction temperatures). The ruggedness of the design can be tested in the following way:

- The IGBT must be turned on at the highest DC-link voltages, collector current and junction temperature (e.g. using the double pulse technique).
- If no fault is generated, the sensitivity of the desaturation protection function can be increased by reducing the capacitance value of C_{ax} and/or reducing the driver supply voltage VDC. This allows the design margin to be checked.

- Alternatively, the turn-on speed on the IGBT module can be artificially reduced by increasing the turn-on gate resistance to check the design margin.

If the design margin is insufficient, it is recommended to increase the response time. Note, however, that the maximum allowed short-circuit time of the IGBT module must not be exceeded under the conditions stated in the data sheet of the IGBT module (if in doubt, please consult the supplier of the IGBT module).

Note that no desaturation protection circuit with sense diodes is recommended for driver cores of voltage classes higher or equal to 3300V.

Disable V_{CEsat} detection by SCALE-2 (excluding 2SC0106T and 2SC0108T)

To disable the V_{CEsat} measurement of gate driver cores, a resistor with a minimum value of 1kΩ needs to be placed between VCEx and COMx.

The reference resistor R_{thx} (if available) may be chosen between 33kΩ and infinity, i.e. the REFx pin may be left open.

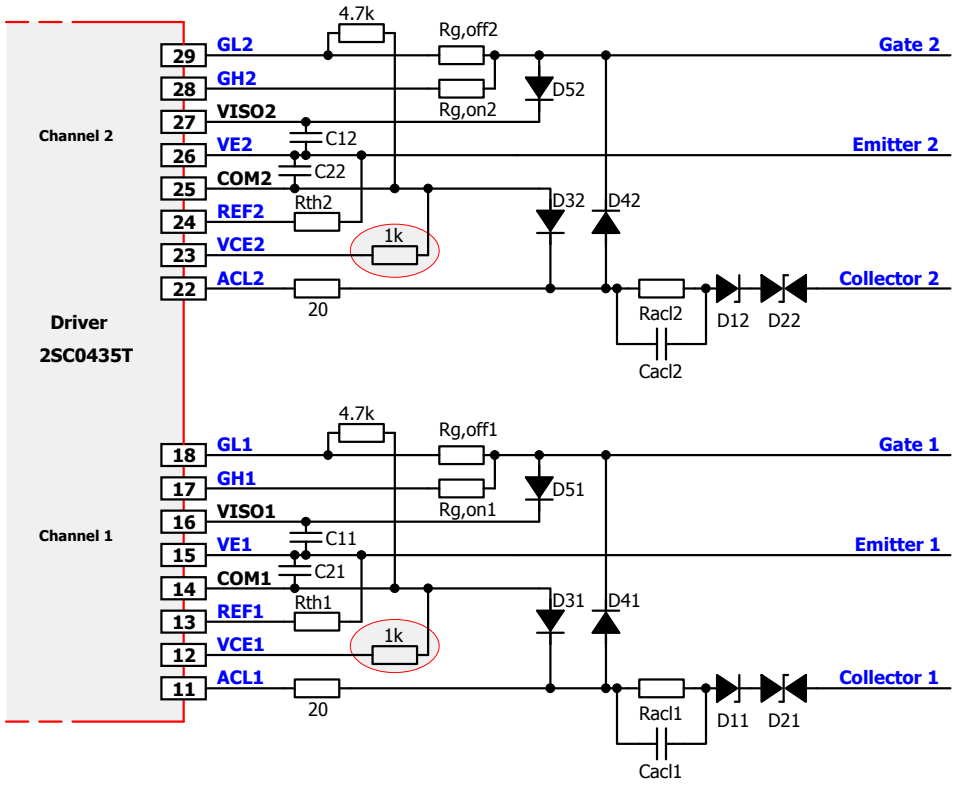

Fig. 19 Disabling the V_{CEsat} detection by SCALE-2 driver cores (example with 2SC0435T)

Disabling the Advanced Active Clamping

To disable the active clamping function, the ACLx input needs to be left open. Refer to the corresponding application manual /1/.

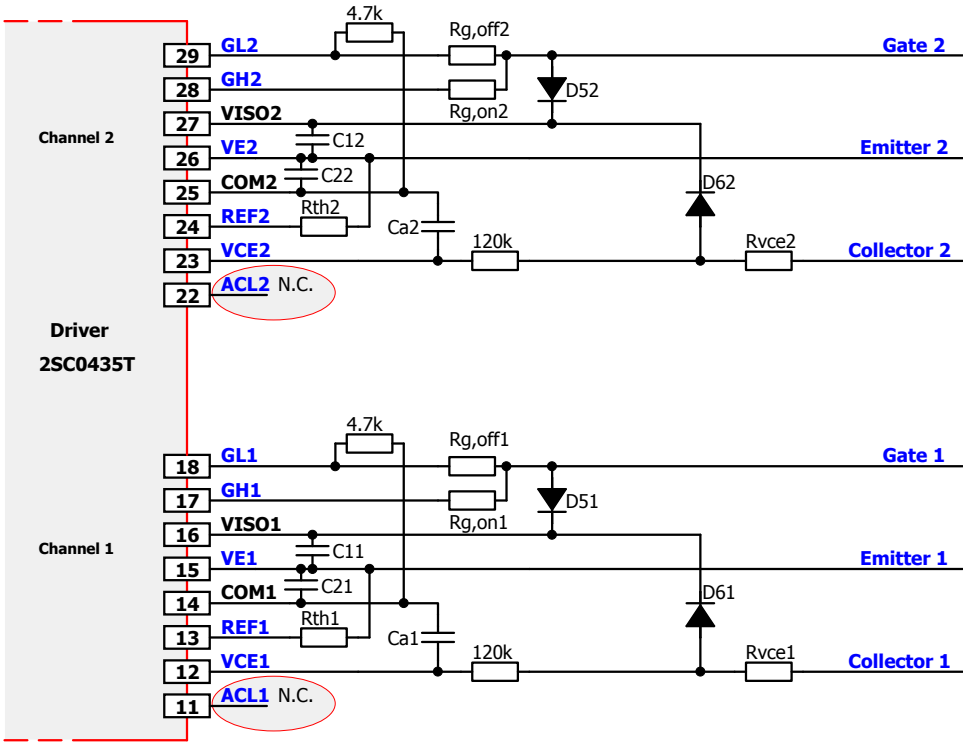

Fig. 20 Disabling Advanced Active Clamping by SCALE-2 (example with 2SC0435T)

Rail-to-rail output and gate voltage clamping

CONCEPT SCALE-2 gate drivers use an N-channel output stage like that shown in Fig. 21. After charging the power semiconductor gate input, the voltage drop over the N-channel MOSFET is nearly zero. SCALE-2 drivers therefore feature rail-to-rail gate outputs.

A rail-to-rail output has several advantages in driving power semiconductors. The first one is that the VISOx voltage can be regulated to 15V. By using a Schottky diode (D_5 in Fig. 21), the gate voltage is clamped to the regulated 15V. This avoids an increase of the external gate-emitter voltage and consequently lowers the IGBT short-circuit current I_{SC} and energy, as the former is highly dependent on the gate-emitter voltage V_{GE}:

$$I_{SC} = f(V_{GE}) \qquad \text{Eq. 11}$$

The gate clamping described here is much more efficient than gate-emitter clamping with transient voltage suppressors. The latter does not allow the gate-emitter voltage to be limited in the short-circuit condition to 15V, as some clamping voltage reserve must be applied in view of the component tolerances and temperature dependence in order to avoid static conduction and therefore overload at V_{GE}=15V.

A second advantage is that parasitic power semiconductor turn-on can be prevented when the gate driver power is off. In that case, the gate-emitter voltage on the power semiconductor is zero. If the collector-emitter voltage V_{CE} increases at a given dV_{CE}/dt, a current I_g will flow in the gate loop via the Miller capacitance C_{Miller}:

$$I_g = C_{Miller} \cdot \frac{dV_{CE}}{dt} \qquad \text{Eq. 12}$$

With the use of D_5 in Fig. 21 the current I_g will charge the blocking capacitors C_{12} and C_{22}. The voltage over C_{12} and C_{22} will generally remain low. A parasitic turn-on of the power semiconductors is therefore not possible. This function can be also used for STO (Safe Torque Operation).

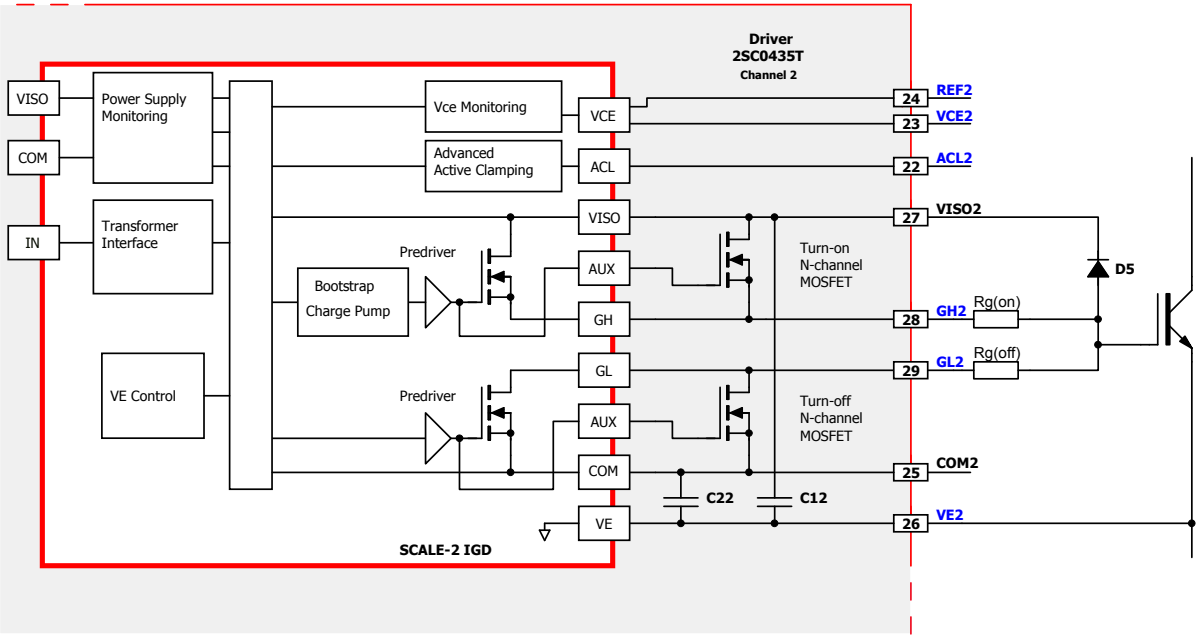

Fig. 21 Rail-to-Rail output and gate clamping (example with 2SC0435T)

Note that the gate clamping described here is not possible on 2SC0108T drivers since VISOx is not available externally. Gate-emitter clamping with transient voltage suppressors should be used instead.

MOSFET mode (not available on 2SC0106T and 2SC0108T)

In IGBT mode, the positive turn-on gate voltage is regulated to 15V and the turn-off gate voltage is negative; typically about -10V for SCALE-2 gate driver cores.

With the MOSFET mode, it is possible to set the turn-off gate voltage to 0V.

It is recommended to proceed in the following way to activate the MOSFET mode on SCALE-2 driver cores:

1) Connect the secondary-side terminals COMx and VEx together. This must be performed with the driver power supply turned off. Otherwise the secondary ASIC IGD may be damaged. The blocking capacitor C_{12} on Fig. 21 may be used if required. The blocking capacitors C_{22} of Fig. 21 are no longer required as they are short-circuited.
2) Select the required gate-emitter voltage at turn-on. The primary-side supply voltage VCC still needs to be 15V. The secondary-side supply voltage VISOx to COMx can be adjusted from 10V to 20V with VDC (exceptions: 2SC0535T and 2SC0635T, see the corresponding application manual /1/). This corresponds to the gate turn-on voltage. The transfer ratio from VDC to VISOx-COMx is typically 1.67. The under-voltage lock-out on the secondary side changes from 12.6V in IGBT mode to 8.75V in MOSFET mode (typical value). A VDC voltage lower than about 5.2V typically produces an under-voltage fault in MOSFET mode. As an example, VDC=6V typically leads to a positive gate turn-on voltage of 10V. Note, however, that this value is dependent on the driver output power and the temperature.
3) The reference voltage V_{th} for V_{CE} monitoring (to be programmed with R_{thx}) must be set at values higher than or equal to 4V referred to COMx.

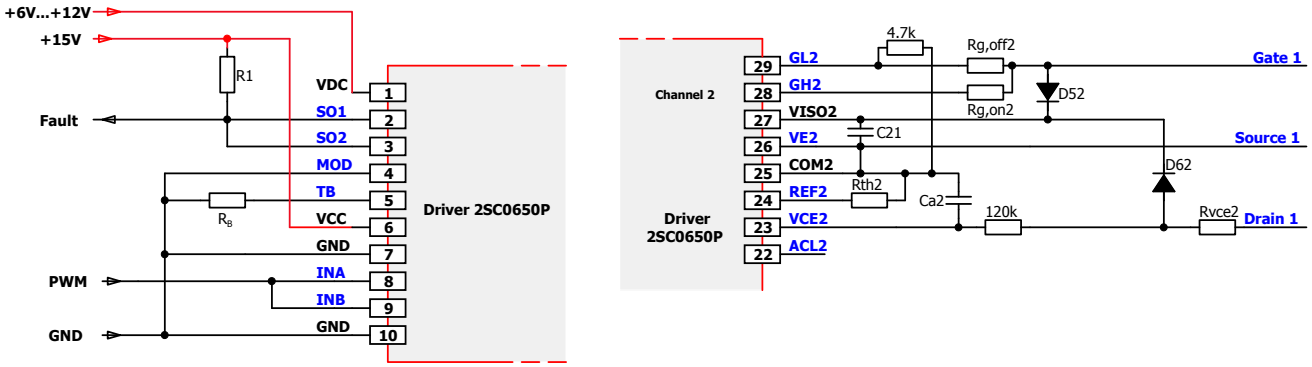

Fig. 22 MOSFET mode (example with 2SC0650P)

Note that the MOSFET mode has been designed for ultra-fast MOSFET switching. The switching delays can thus be reduced to a minimum. A single positive turn-on voltage is then necessary.

MOSFETs have low gate-source threshold voltages. The use of MOSFET mode is consequently not always recommended and depends on the application. The IGBT mode can be used to drive MOSFETs and avoid their parasitic turn-on thanks to the negative gate-source voltage in the off-state.

Paralleling a dual-channel driver to a single output (not available on 2SC0106T)

Dual-channel driver cores can be configured to a single driver core with the double output power and gate current (exception 2SC0106T).

It is recommended to proceed in the following way and as shown in Fig. 23 to merge both driver channels to one logical channel (excluding 2SC0108T):

- Direct mode must be selected (MOD pin pulled to GND).
- Both input signals INA and INB must be connected together.
- Both secondary-side emitter potentials VE1 and VE2 must be connected together.
- It is recommended to disable the desaturation protection for one channel while it is enabled on the other channel.
- If available, the reference value V_{th2} is set up to 10V with R_{th2}=68kΩ.
- Both channels need gate resistors to decouple the driver output stages. The driver channels are connected together on the IGBT gate side of the gate resistors. The turn-on and turn-off gate resistors need to be the same for both channels with a tolerance value of ≤5% (1% recommended).
- The active clamping controls the turn-off driver stages in the driver core at turn-off. Each of the Advanced Active Clamping pins ACLx of both channels must therefore be connected to a 20Ω resistor according to Fig. 23 (The 20Ω resistors as well as D_{3x} must be omitted on 2SC0635T, as these components are already available on the driver core).
- Both fault signals SO1 and SO2 can be connected to a single fault signal SO.
- As soon as a fault is detected at SO, the PWM input signal must be pulled to GND in order to turn-off any driver channel that may not already be turned off. Omitting this point could lead to thermal damage to the driver, as one driver channel is turned off in the fault condition and the other remains turned on, leading to high power losses in the driver. The PWM input should not be activated before the SO fault signal is high again, i.e. no fault signal is available. This is important in order to avoid only one channel switching, as the blocking time of both driver channels is not exactly the same. Additional restrictions may apply when using 2SC0635T if the CSHDx pin is used (see the corresponding application manual /1/).

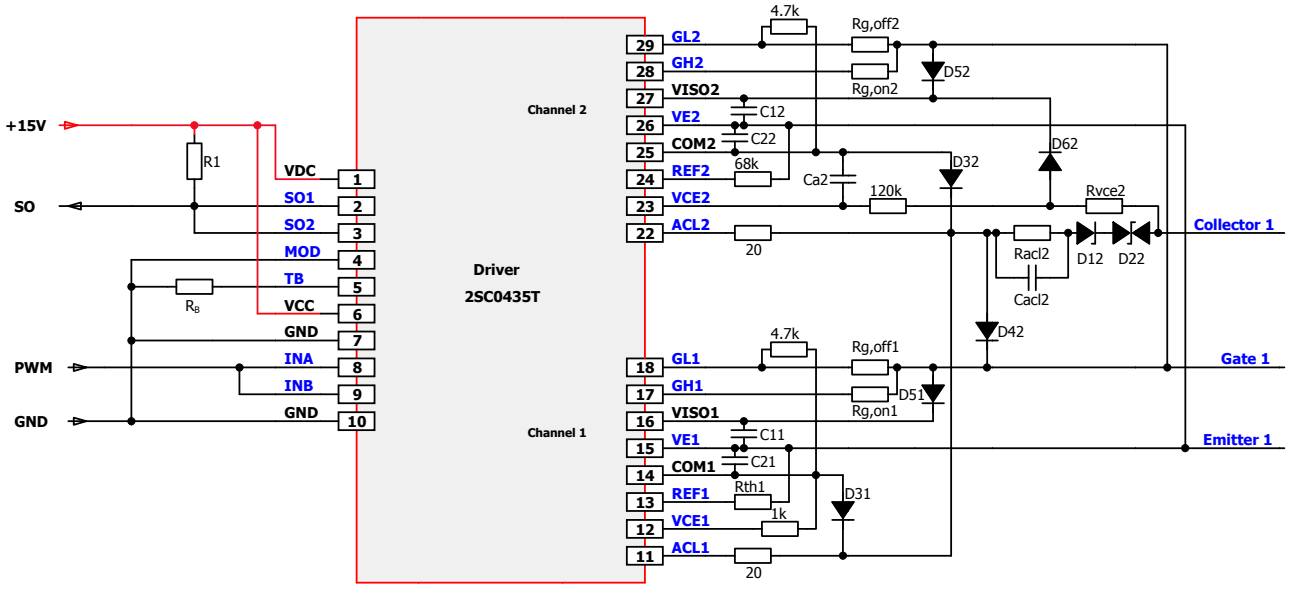

Fig. 23 Paralleling a dual-channel driver to a single output (example with 2SC0435T)

Paralleling the two gate driver channels on 2SC0108T is similar to the procedure for all other SCALE-2 gate driver cores. The main difference is that no Advanced Active Clamping is available. If (basic) active clamping is used, the transient voltage suppressor chain is connected directly to the gate (see Fig. 24).

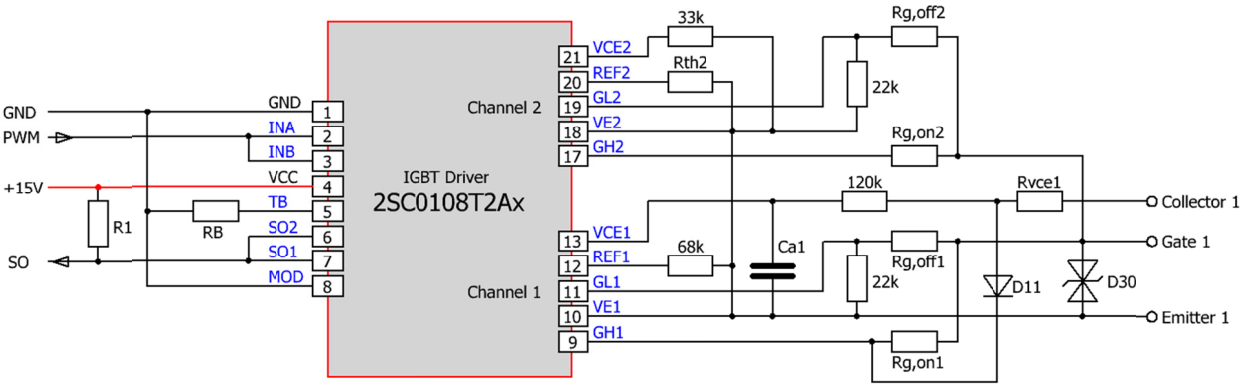

Fig. 24 Paralleling both driver channels of 2SC0108T

Note that the two gate driver channels of 2SC0106T cannot be run in parallel.

Disabling one channel for chopper applications

In some cases, a single gate driver is required, such as for chopper operation, e.g. a break chopper in a DC-link bus. A single gate driver is not always available or commercially viable for such applications. A dual-channel gate driver core can therefore be used where one channel has to be disabled.

It is recommended to proceed in the following way to disable one driver channel:

- The corresponding signal input INx must be pulled to GND.
- The fault feedback SOx can be left open.
- Direct mode (if available) must be selected (MOD pin pulled to GND).
- The secondary side of the channel can be left open (not connected).

Position of the Gate Driver in the Converter

The temperature as well as both magnetic and electric fields can influence the functionality of the signal electronics. Choosing the right position for the gate driver in the power electronics system helps to prevent system dysfunction and EMI effects.

CONCEPT SCALE-2 gate drivers are generally designed for ambient temperatures of up to 85°C. Excessive temperatures mainly limit the DC/DC power. In the worst case, the DC/DC transformer core goes into saturation and the gate driver core is destroyed. In converters where the gate driver is placed close to the heat sink or the power semiconductors, it is important to check that the maximum permissible temperature around the driver is not exceeded.

Furthermore, high currents generate high magnetic fields and high voltages generate high electric fields. Combined with high switching speeds, these fields represent a harsh environment for the signal electronics available on the gate drivers. This point is further detailed below.

Driver placement on top of 17mm IGBT modules or close to high magnetic fields

17mm IGBT modules are becoming increasingly popular in power electronics applications. Manufacturers like Danfoss Silicon Power, Fuji, Infineon, IXYS, Mitsubishi and Semikron offer a range of 17mm packages on the market.

It is not recommended to use most of the SCALE-2 driver cores (exceptions see below) directly on top of IGBT modules, and especially not on top of 17mm IGBT modules. Magnetic field coupling during turn-on and turn-off events and especially during IGBT short circuit can lead to malfunction of the driver.

Some SCALE-2 driver cores have been optimized to work in environments with high magnetic fields. They can be used directly on top of IGBT modules without problems. These drivers are:

- 2SC0106T – the entire driver family
- 2SC0108T2D0-07 and 2SC0108T2D0-12
- 2SC0435T2F0-17
- 2SC0650P – the entire driver family
- 1SC2060P – the entire driver family
- 1SC0450V – the entire driver family

AC and DC bus bar

Laminated DC bus bars generally produce low external magnetic and electric fields due to their laminated structure. A gate driver can therefore be located on top or underneath the DC bus as long the insulation or the clearances are sufficient.

However, the situation concerning the AC or phase leg bus bar is different. The output current generates a magnetic field around the bus bar and the rate of change of the electric field is generally high. If the gate driver is placed directly underneath or above the AC bus bar, shielding may be necessary. This can be an iron plate (shielding for low frequencies) or a thick aluminum or copper plate (shielding for high frequencies). The eddy current flowing in the shield will partially compensate for the magnetic field generated near the gate driver.

However, it is usually recommended to maintain a minimum distance (several cm are generally sufficient) between the AC bus bar and the gate driver core to reduce the effect of the magnetic field on the driver.

Generally speaking, the closer the conducting current and the signal electronics are to each other, the higher is the risk of electromagnetic influences.

PCB Layout

SCALE-2 driver cores are sophisticated products that require properly designed PCB layouts in order to work efficiently and to deliver full performance. Stripboards ("Veroboards") must therefore not be used together with SCALE-2 driver cores. It is usually recommended to use 4-layer PCBs. Two-layer PCBs may also be used, but the performance and/or flexibility are then reduced.

PCB thickness

CONCEPT recommends using a PCB thickness of 1.55mm or higher. The typical pin length of 2.54mm of many of the SCALE-2 driver cores has been optimized for the use of 1.55mm PCB thickness.

It is recommended to use drivers with longer pins when using PCB thicknesses of 2mm or higher to avoid soldering problems during production. The following drivers have long pins (5.84mm):

- 2SC0108T2C0-17, 2SC0108T2F0-17
- 2SC0435T2C0-17, 2SC0435T2E0-17, 2SC0435T2F0-17
- 2SC0650P2C0-17
- 1SC2060P2A0-17
- 2SC0535T2A0-33
- 2SC0635T2A0-45
- 1SC0450V2A0-45, 1SC0450V2A0-65

Separation of areas with different high-voltage potentials

One important rule for PCBs designed for power electronics applications is that layers relating to different high-voltage potentials must never overlap as shown in Fig. 25. If this is omitted, large coupling capacitances between the different high-voltage potentials will result, leading to excessive common-mode current I_{com} on the PCB during switching operation. Moreover, the long-term isolation reliability may become problematic.

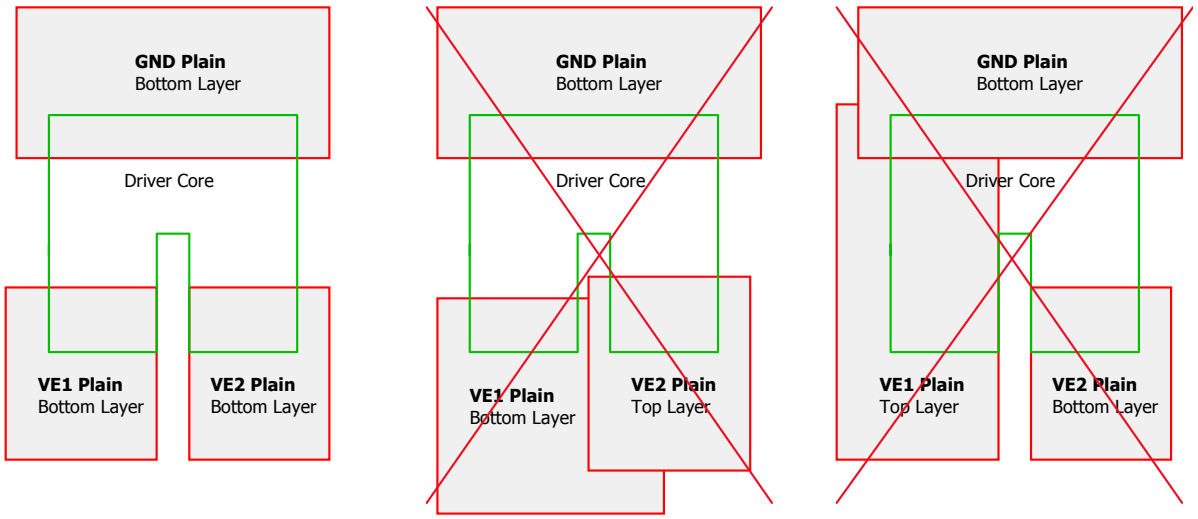

Fig. 25 PCB layout of SCALE-2 driver adapter boards

Equations 13 and 14 describe how to calculate common-mode currents I_{com} relating to overlapping plains in different PCB layers during IGBT commutation with a rate of change of the collector-emitter voltage of dV_{CE}/dt:

$$C_{PCB} = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{l}$$ Eq. 13

A is the area where high-voltage potentials overlap, l is the distance between both PCB layers, ε_r=5, and ε_0=8.85pF/m.

$$I_{com} = C_{PCB} \cdot \frac{dV_{ce}}{dt}$$ Eq. 14

Not only planes (e.g. ground or emitter potentials) are affected by these rules. All other signal lines with large switching potential differences must also satisfy this rule. A high-side collector potential must therefore – as an example – never cross a low-side gate signal on the PCB layout.

It is mandatory to implement sufficient clearance and creepage distances as required by the corresponding standards (see also section "Clearance and creepage distances for PCBs ").

Use of planes

It is highly recommended to use planes to distribute constant potentials (especially power supplies and ground) efficiently over the corresponding PCB areas. Additionally, the planes act as magnetic shielding and strongly reduce the influence of external magnetic fields if they are properly designed.

The layers can be used in the following way (example):

Driver primary side

- Top Layer: Components, cooling surface and traces
- Mid Layer 1: VCC
- Mid Layer 2: VDC
- Bottom Layer: GND, cooling surface and test points

Driver secondary side(s)

- Top Layer: Components, cooling surface and traces
- Mid Layer 1: Emitter or VISO
- Mid Layer 2: VISO or emitter
- Bottom Layer: COM, cooling surface and test points

Several planes with different potentials (example emitter and COM) may naturally also be located on the same layer, if required. Additional planes with other stable potentials, if available (5V, -15V, …), may also be established.

On the other hand, it is impermissible to build planes with changing potentials, as such planes will generate coupling capacitances leading to corresponding current flows when potentials are changing. It is also impermissible to locate planes over areas with changing high-voltage potentials: the complete resistor chain of the desaturation protection function as well as all TVS for Advanced Active Clamping must always remain free from planes.

Clearance and creepage distances for PCBs

Tab. 1 gives an overview of the required clearance and creepage distances for several IGBT voltage classes. Several widely used standards are considered. The listed data assumes Pollution Degree 2 (PD2), Overvoltage Category II (OV II) and standard FR4 PCB material of material category IIIa.

Note that the working voltages given in Tab. 1 do not necessarily correspond those used to design the corresponding driver cores. Please check the creepage distances given in the specific data sheets /2/.

Voltage class of power module (V_{CES})	Standard	System voltage	Working voltage	Max. altitude of operation	Impulse voltage for functional insulation	Impulse voltage for reinforced insulation	Min. clearance distance for functional insulation	Min. clearance distance for reinforced insulation	Min. creepage distance for functional insulation[1)]	Min. creepage distance for reinforced insulation[1)]
600V	EN 50178 1997-07	$424V_{RMS}$	$400V_{DC}$	2000m	3121V	4994V	2.1mm	4.2mm	2.1mm	4.2mm
650V		$460V_{RMS}$	$400V_{DC}$		3298V	5277V	2.3mm	4.6mm	2.3mm	4.6mm
1200V		$849V_{RMS}$	$800V_{DC}$		5243V	8388V	4.6mm	8.7mm	4.6mm	8.7mm
1700V		$1202V_{RMS}$	$1200V_{DC}$		6808V	10893V	6.5mm	12.3mm	6.5mm	12.3mm
3300V		$2333V_{RMS}$	$2500V_{DC}$		11334V	18134V	13.0mm	22.8mm	13.0mm	25.0mm
4500V		$3182V_{RMS}$	$3400V_{DC}$		14667V	23468V	18.0mm	30.9mm	18.0mm	34.0mm
6500V		$4596V_{RMS}$	$4500V_{DC}$		19853V	31764V	25.5mm	45.5mm	25.5mm	45.5mm
600V	IEC 60077-1 Ed. 1 1999-10	$424V_{RMS}$	$400V_{DC}$	1400m	4000V	6400V	3.0mm	8.0mm	4.0mm	8.0mm[2)]
650V		$460V_{RMS}$	$400V_{DC}$		4000V	6400V	3.0mm	8.0mm	4.0mm	8.0mm[2)]
1200V		$849V_{RMS}$	$800V_{DC}$		5000V	8000V	4.0mm	8.0mm	8.0mm	8.0mm[2)]
1700V		$1202V_{RMS}$	$1000V_{DC}$		8000V	12800V	8.0mm	18.0mm	10.0mm	18.0mm[2)]
3300V		N.a.[3)]								
4500V		N.a.[3)]								
6500V		N.a.[3)]								
600V	IEC 60664-1 Ed. 2 2007-04	$424V_{RMS}$	$400V_{DC}$	2000m	4000V	6000V	3.0mm	5.5mm	3.0mm	5.5mm
650V		$460V_{RMS}$	$400V_{DC}$		4000V	6000V	3.0mm	5.5mm	3.0mm	5.5mm
1200V		$849V_{RMS}$	$800V_{DC}$		6000V	8000V	5.5mm	8.0mm	5.5mm	8.0mm
1700V		$1000V_{RMS}$	$1000V_{DC}$		6000V	8000V	5.5mm	8.0mm	5.5mm	10.0mm
3300V		N.a.[3)]								
4500V		N.a.[3)]								
6500V		N.a.[3)]								
600V	IEC 61800-5-1 Ed. 2 2007-07	$424V_{RMS}$	$400V_{DC}$	2000m	4000V	6000V	3.0mm	5.5mm	3.0mm	5.5mm
650V		$460V_{RMS}$	$400V_{DC}$		4000V	6000V	3.0mm	5.5mm	3.0mm	5.5mm
1200V		$849V_{RMS}$	$800V_{DC}$		6000V	8000V	5.5mm	8.0mm	5.5mm	8.0mm
1700V		$1202V_{RMS}$	$1200V_{DC}$		6777V	10844V	6.5mm	12.3mm	6.5mm	12.3mm
3300V		$2333V_{RMS}$	$2500V_{DC}$		11129V	17806V	12.7mm	22.0mm	25.0mm	50.0mm
4500V		$3182V_{RMS}$	$3400V_{DC}$		14392V	23028V	17.3mm	30.3mm	34.0mm	68.0mm
6500V		$4596V_{RMS}$	$4500V_{DC}$		19597V	31356V	24.5mm	44.9mm	45.0mm	90.0mm

1) If the determined creepage distance is smaller than the respective clearance distance for functional or reinforced insulation, the clearance distance will be chosen for this particular creepage distance for safety reasons.

2) IEC 60077-1 does not distinguish between functional and reinforced insulation with respect to the creepage distances. The value of the functional insulation is therefore used for reinforced insulation as long as the respective clearance distance for reinforced insulation is not higher (see also previous footnote).

3) N.a.: Not applicable

Tab. 1 Summary of required creepage and clearance distances according to several standards

Gate driver cores in applications at higher altitudes

The creepage and clearance distances of CONCEPT gate driver cores are determined according to specific standards (see product documentation /1/, /2/), which indicate a maximum altitude of operation (see also Tab. 1).

For use of the drivers at higher altitudes, correction factors for the clearances are usually given in the standards and must be considered.

For example, for an IGBT power module in a voltage class of 1700V, the maximum altitude for a 2SC0108T driver is 2000m. If the application operates at higher altitudes and the corresponding standards must be satisfied, the maximum permissible system voltage must be reduced, or else the next larger CONCEPT IGBT

gate driver is required. Thus, 2SC0435T drivers can operate according to the standards up to an altitude of 2900m.

Note that neglect of these requirements can lead to destruction of the IGBT drivers and IGBT modules.

CONCEPT base boards

CONCEPT has developed the following base boards to show how correct layouts for the driver cores can be realized:

2BB0108T for 2SC0108T (see www.igbt-driver.com/go/2BB0108T)

2BB0435T for 2SC0435T (see www.igbt-driver.com/go/2BB0435T)

2BB0535T for 2SC0535T (see www.igbt-driver.com/go/2BB0535T)

Schematics, BOM and even the Gerber files of the layouts are available on the specified Internet pages.

Fig. 26 and Fig. 27 show examples of base board layouts.

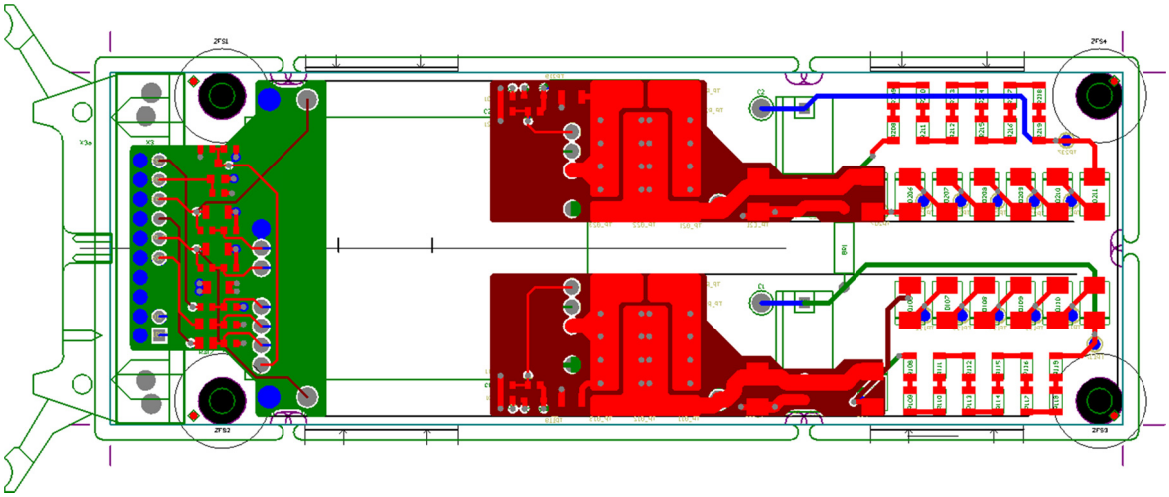

Fig. 26 PCB layout of CONCEPT base board 2BB0108T

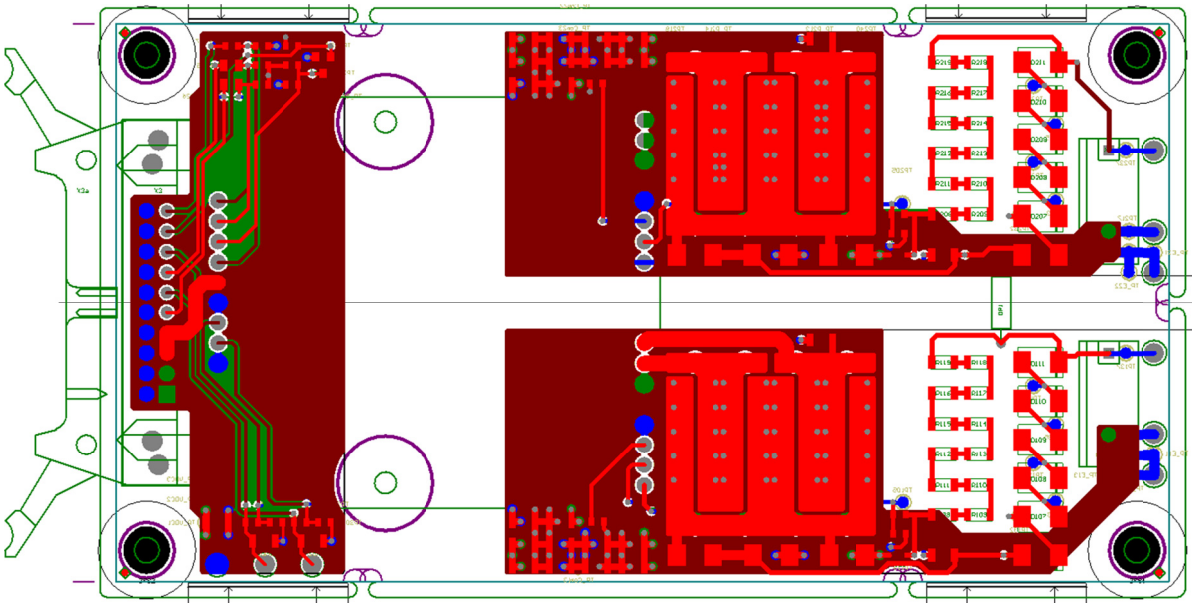

Fig. 27 PCB layout of CONCEPT base board 2BB0435T

Typical Application Failures

Impact on the driver	Effect	Cause	Corrective Action
Primary-side DC/DC MOSFET destroyed or LDI ASIC destroyed (2SC0108T)	DC/DC overload	• Excessive switching frequency • High noise on INA or INB • Partial discharge • Short circuit in gate, emitter, VEx, VISOx or COMx • Use of oversized gate/emitter capacitor C_{GE} • Excessive gate charge Q_g • LC gate oscillation • Excessively high ambient temperature • Defective ceramic capacitor	• Select next powerful gate driver or reduce switching frequency • EMI protection e.g. minimum pulse suppression • Mostly PCB layout failure; check all clearance and creepage distances • Assembly or layout failure • Calculate the power losses for C_{GE} • Calculate the power losses for Q_g • Remove excessive inductance in the gate loop • Reduce the ambient temperature below 85°C • Avoid mechanical damage by handling process or bending of PCB
LDI ASIC destroyed		• VDD>16V • Pull-up resistor value at SOx too small • ESD handling • Max. isolation voltage of 1700V exceeded	• Limit VDD to 16V • Increase the resistor value • Improve ESD handling • Reduce V_{CE} overvoltage e.g. with active clamping or change to a higher IGBT blocking voltage
IGD ASIC destroyed	Excessive Advanced Active Clamping feedback (>3µs)	• Excessive DC-link voltage • Excessive stray inductances	• Overall design failure, change to higher IGBT blocking voltage • Improve the DC bus bar (reduced stray inductance); do not apply current >40mA (mean value) to the ACLx pin
IGD ASIC destroyed		• VISOx > 30V	• Limit VDC to 16V
Short circuit with destruction of LDI, IGD or DC/DC MOSFET	Crack of ceramic capacitors	• Handling process, mechanical destruction; can also happen in final mechanical assembly process	• Careful mechanical handling and assembly process
Delay divergence of gate signals between parallel connected IGBTs (>25ns) or jitter >5ns	Increased initial propagation delay	• Use of half-bridge mode • Slow rise and fall times applied to driver inputs	• Use of direct mode • Insert Schmitt-trigger gates to INA/INB

Bibliography

/1/ Description and Application Manual of SCALE™-2 driver cores, CONCEPT

/2/ Data sheets of SCALE™-2 driver cores, CONCEPT

/3/ Application Note AN-0901: Methodology for Controlling Multi-Level Converter Topologies with SCALE™-2 IGBT Drivers, CONCEPT

/4/ Application Note AN-0904: Direct Paralleling of SCALE™-2 Gate Driver Cores, CONCEPT

/5/ Paper: Safe Driving of Multi-Level Converters Using Sophisticated Gate Driver Technology, PCIM Asia, June 2013

Note: The Application Notes are available on the Internet at www.igbt-driver.com/go/app-note and the papers at www.IGBT-Driver.com/go/paper

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